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LiveWebcast

How to Make Designing Photonic Integrated Chips Accessible and Affordable

September 16, 2014

7pennies Dedicated Consulting · BRIGHT Integrated PHOTONICS · JePPIX · LioniX (Our chips enable your products) · Mentor Graphics · PhoeniX Software

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How to Make
Designing Photonics Integrated Chips Accessible and Affordable

16-Sep-2014

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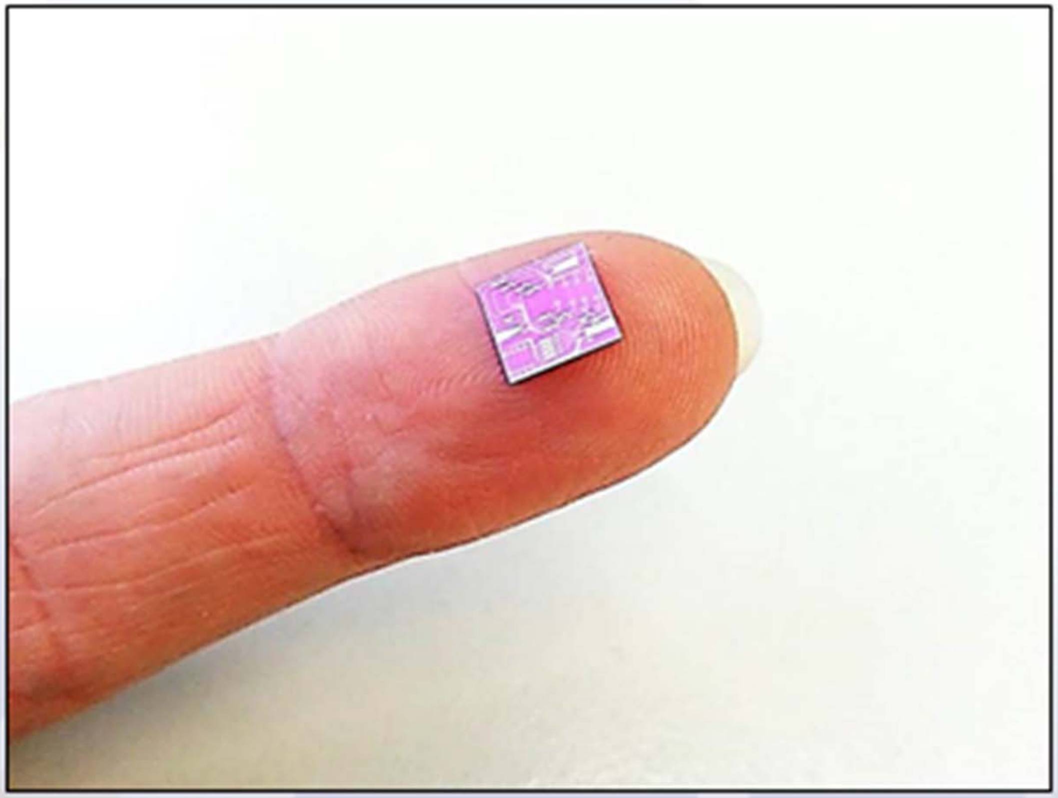
Agenda

- Introduction on PICs
- Multi-Project Wafer (MPW) shuttle for Photonics
- Photonic Process Design Kits (PDK)
- Choosing between different material systems for PICs
- Packaging, scaling to full production, and IP
- Conclusions
- Sponsors:
- Organizers:

Introduction to photonic ICs

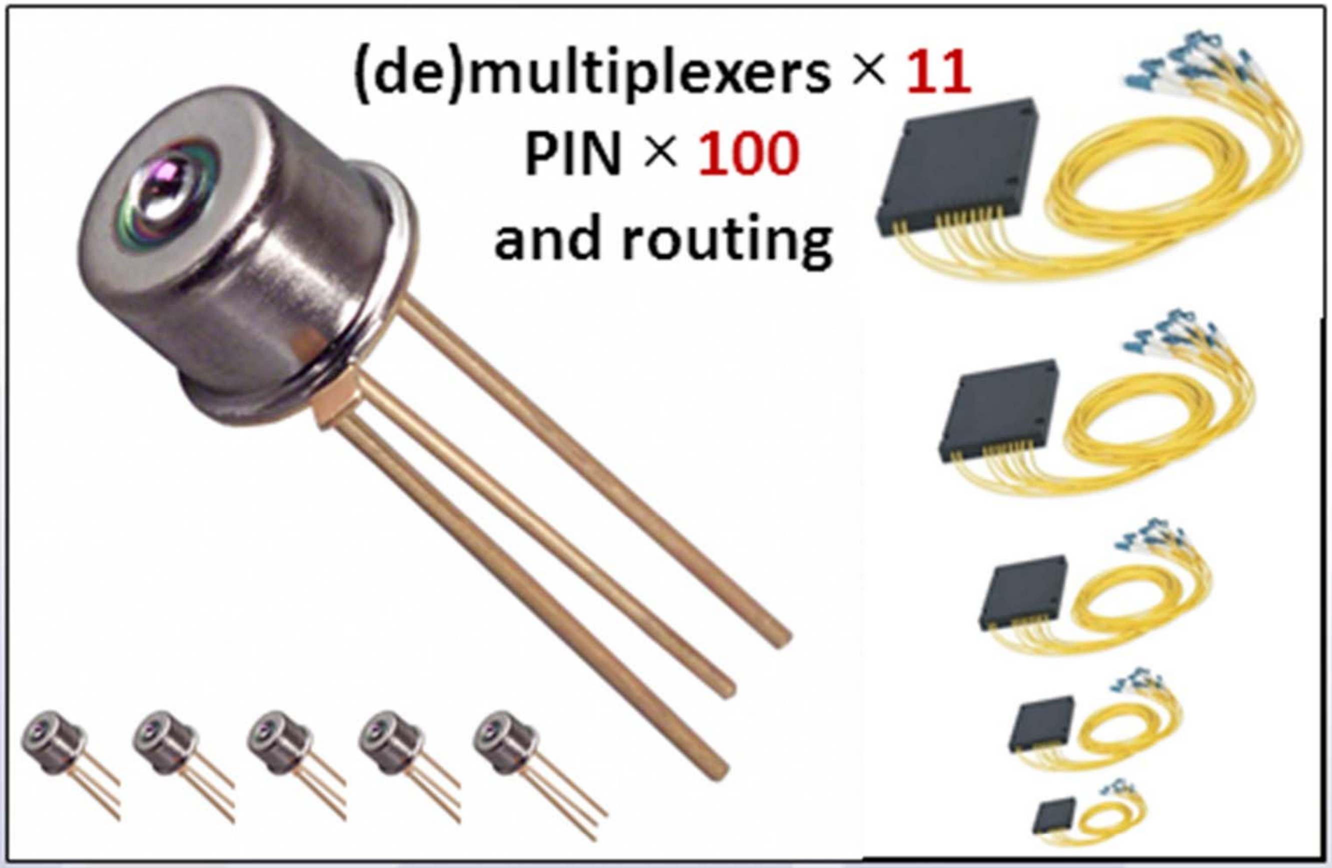
- What is inside of photonic ICs?



- light propagation
- amplification and light generation
- fast modulation

Introduction to photonic ICs

- What is inside of photonic ICs?



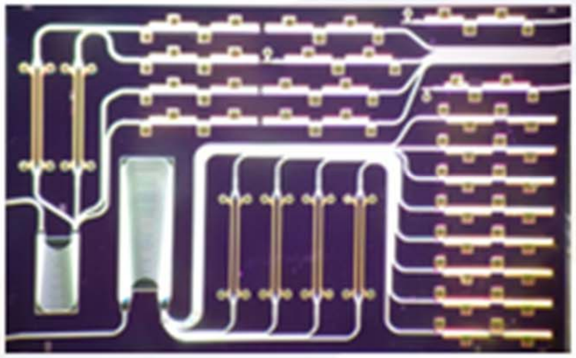
Single Photonic
Integrated Circuit

6 mm × 8 mm
FBG sensor unit

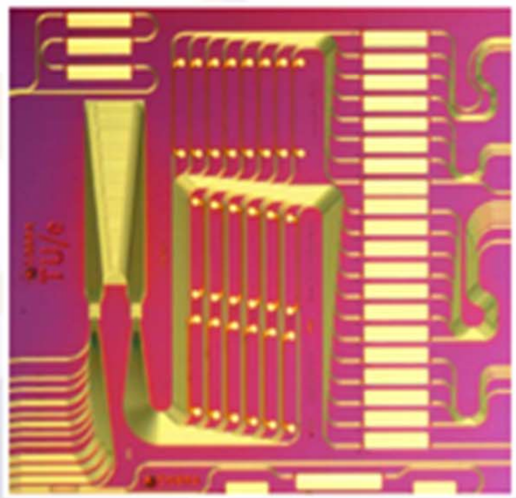
conventional **vs.** **integrated**

Application specific photonic ICs

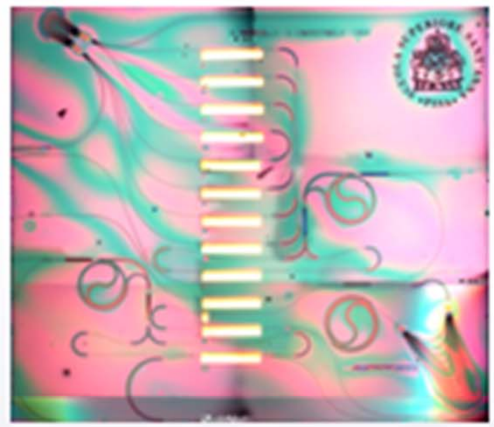
Fiber to the Home
Wireless



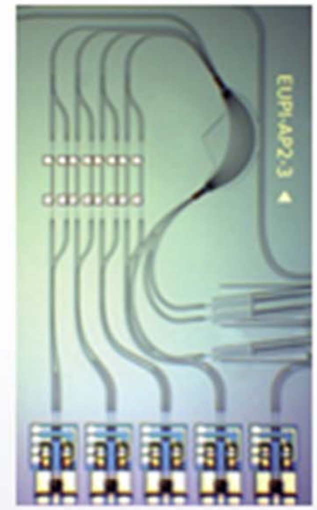
Medical
Bio-imaging



Datacom
Switching

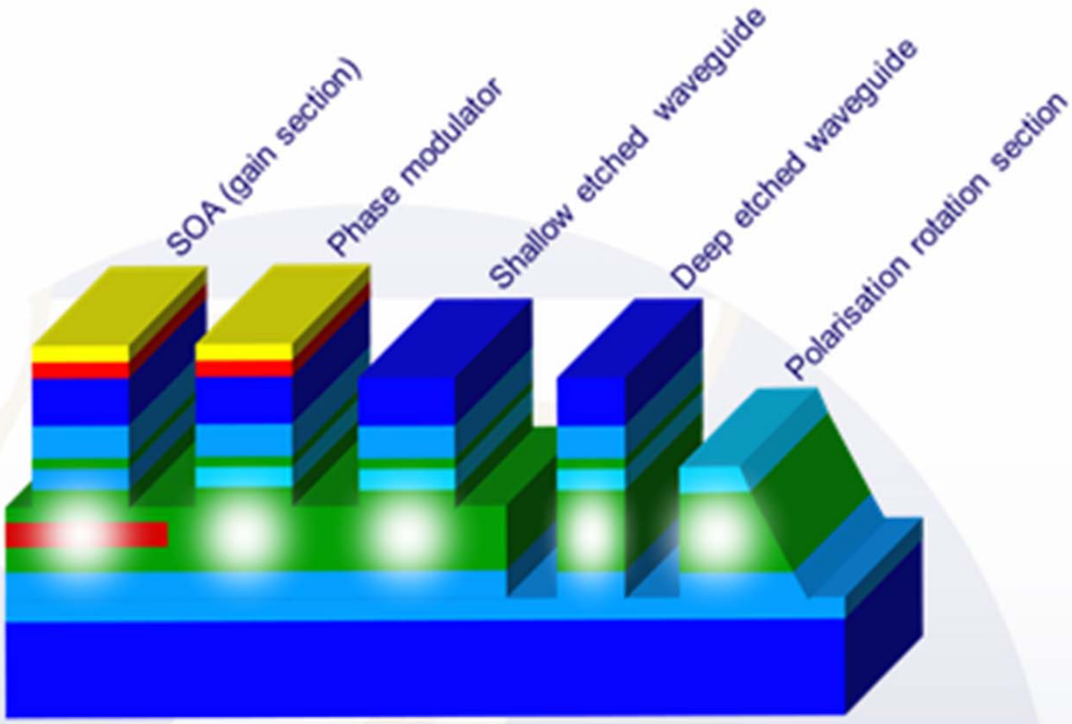


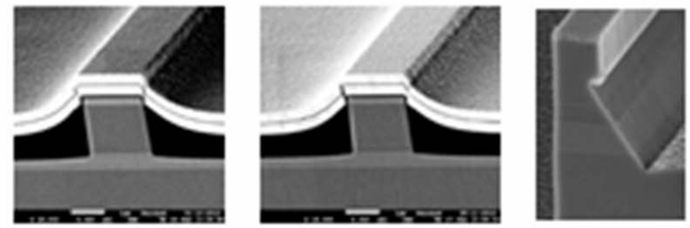
Sensor
Readouts



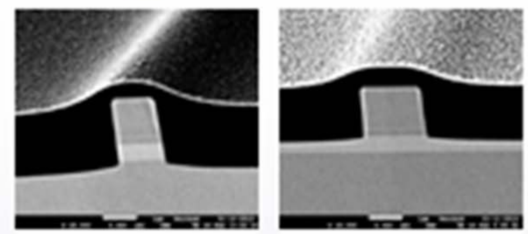
- Application driving technology ?
  - Too expensive, need for high volume market!
  - Fragmentation, long-time investment

Generic foundry model



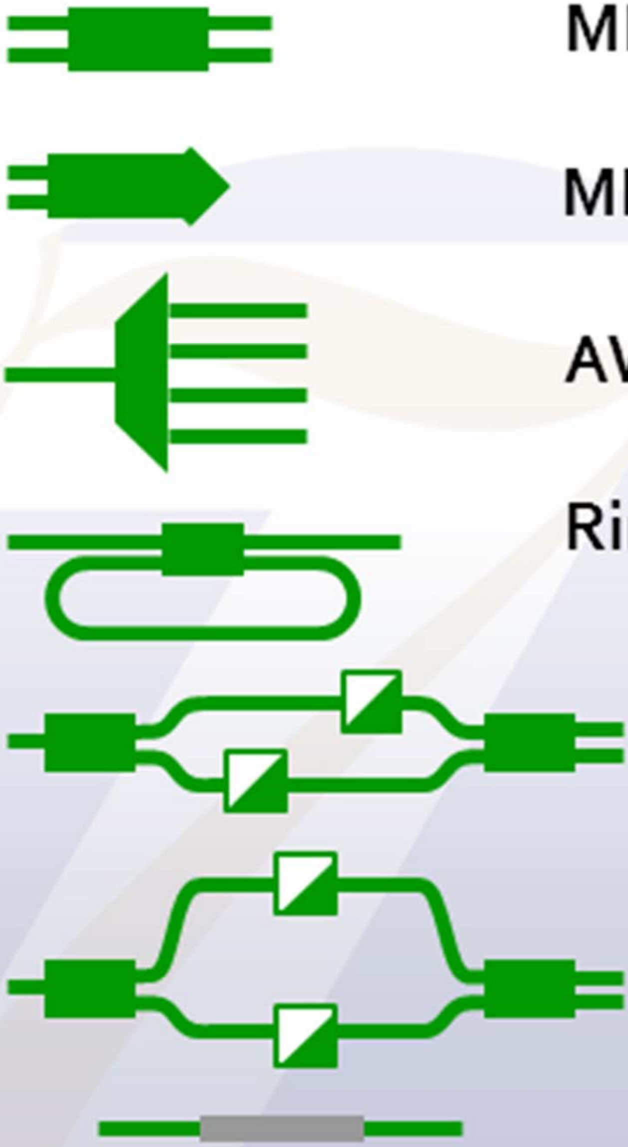


Building blocks!



- Solution: generic technology!
  - Cost sharing, application separated from technology development, fast prototyping
  - Verified components (building blocks): reduction of design time and number of fab cycles

Generic technology: building blocks



MMI-couplers and filters

MMI-reflectors

AWG-demux

Ring filters

Polarisation splitters
Polarisation combiners

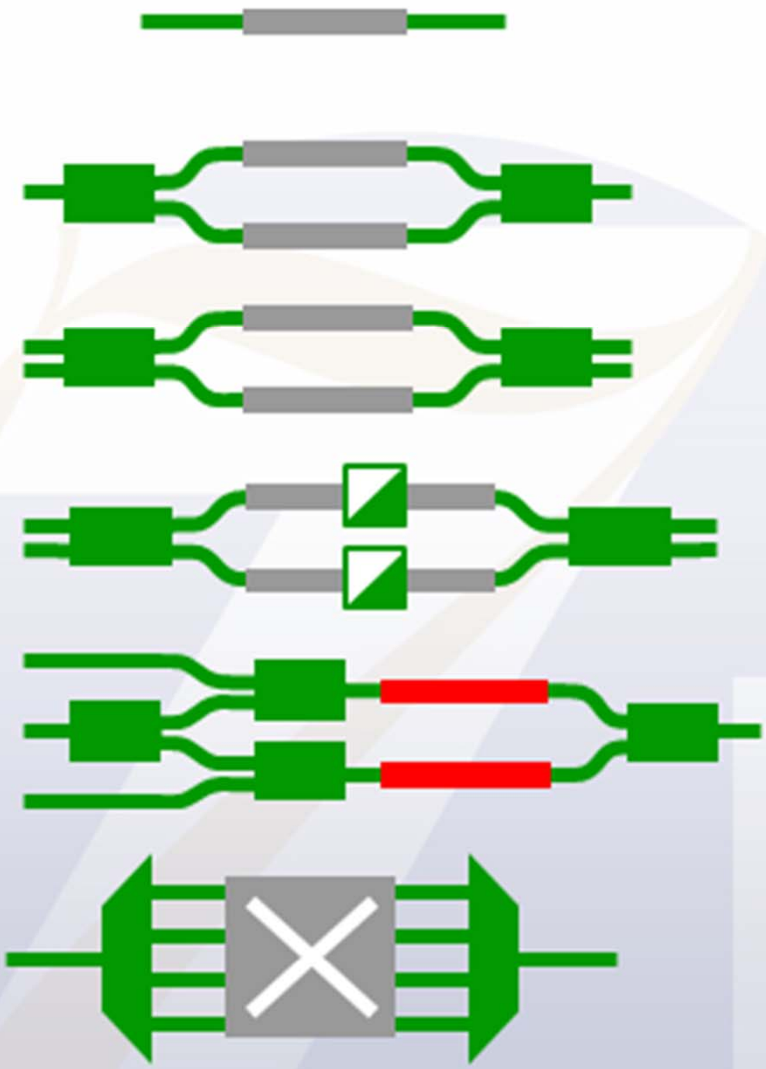
Polarisation independent differential delay lines

Thermo optic Phase modulator

Passive devices

InP
Silicon
TriPleX

Generic technology: building blocks



Phase modulator

Amplitude modulator

Fast space switch

Polarisation
independent 2x2 switch

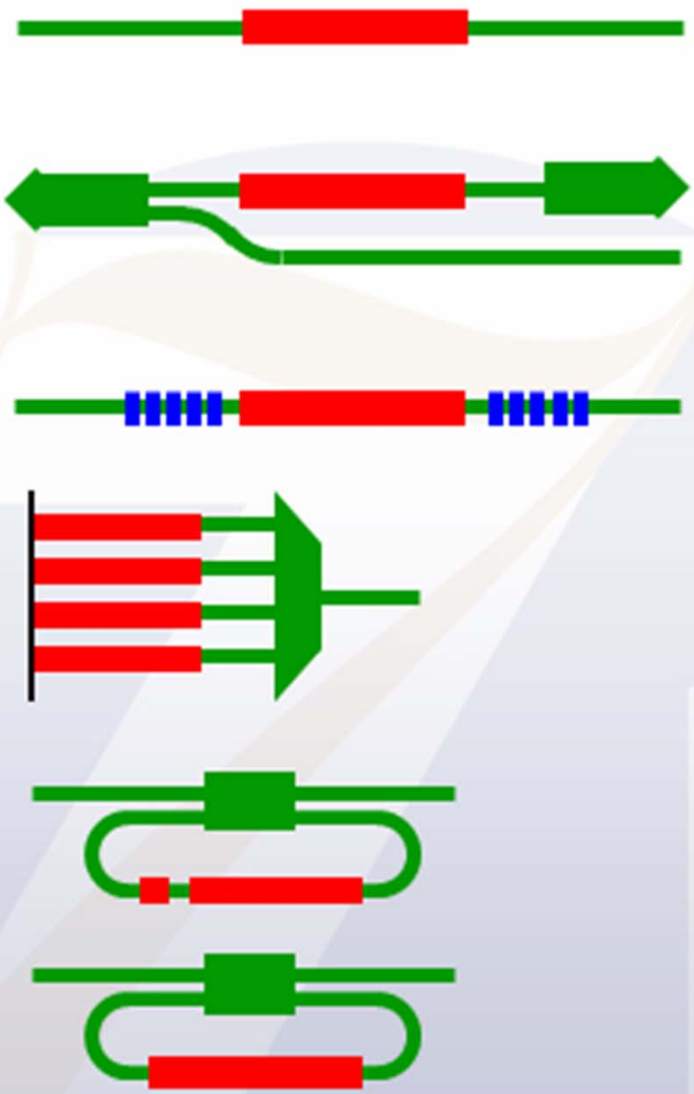
Ultrafast switch

WDM crossconnect
WDM add-drop

Switches
Modulators

InP
Silicon

Generic technology: building blocks



SOA

Fabry-perot lasers

Tunable DBR lasers

Multiwavelength lasers

Picosecond pulse laser

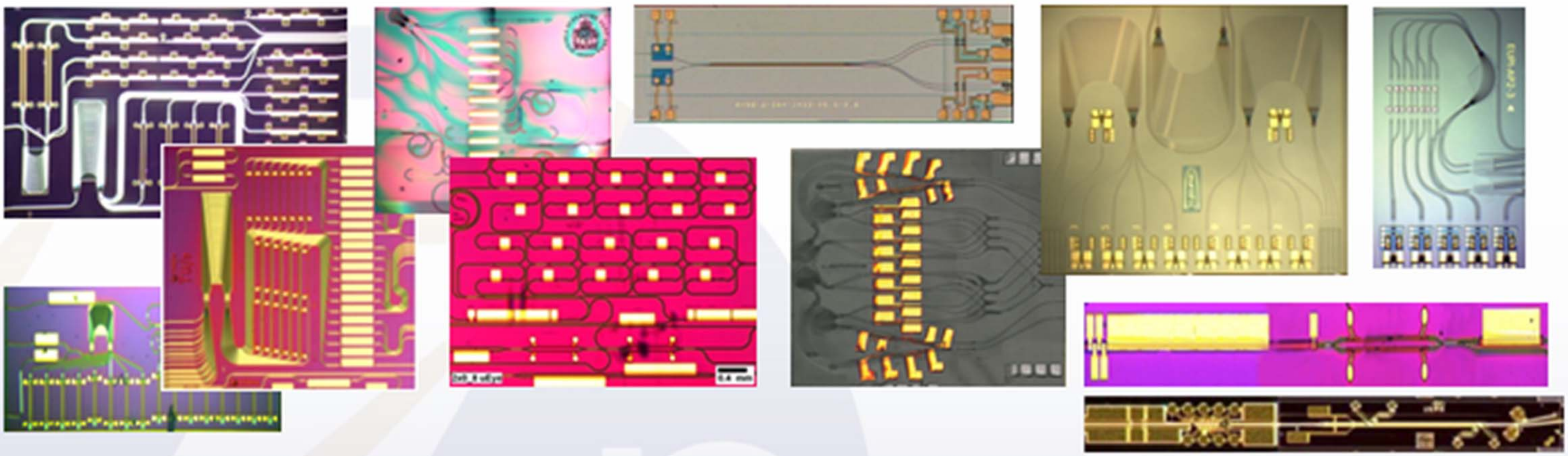
Ring lasers

Lasers

InP

Generic foundry model

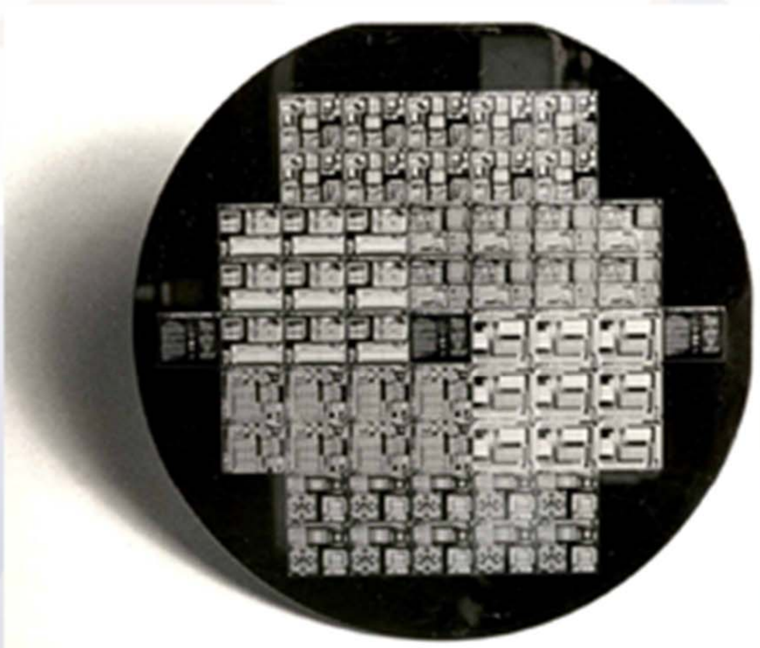
350+ ASPICs developed in generic fabs via MPW runs



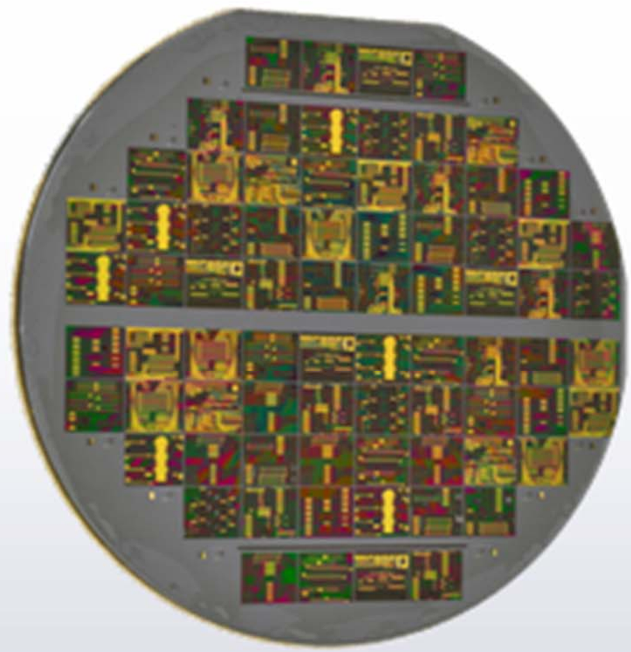
- Photonic advanced PDK with BBs available for layout and simulation, just like for electronics and CMOS designers
- Photonic ASICs fabricated using the same processes, using existing commercial manufacturing lines (towards volume production)

Multi-project wafer runs

- Sharing wafer : sharing fab costs
  - simple and cheap way of prototyping
  - fabless business model



Silicon electronic ICs 1979

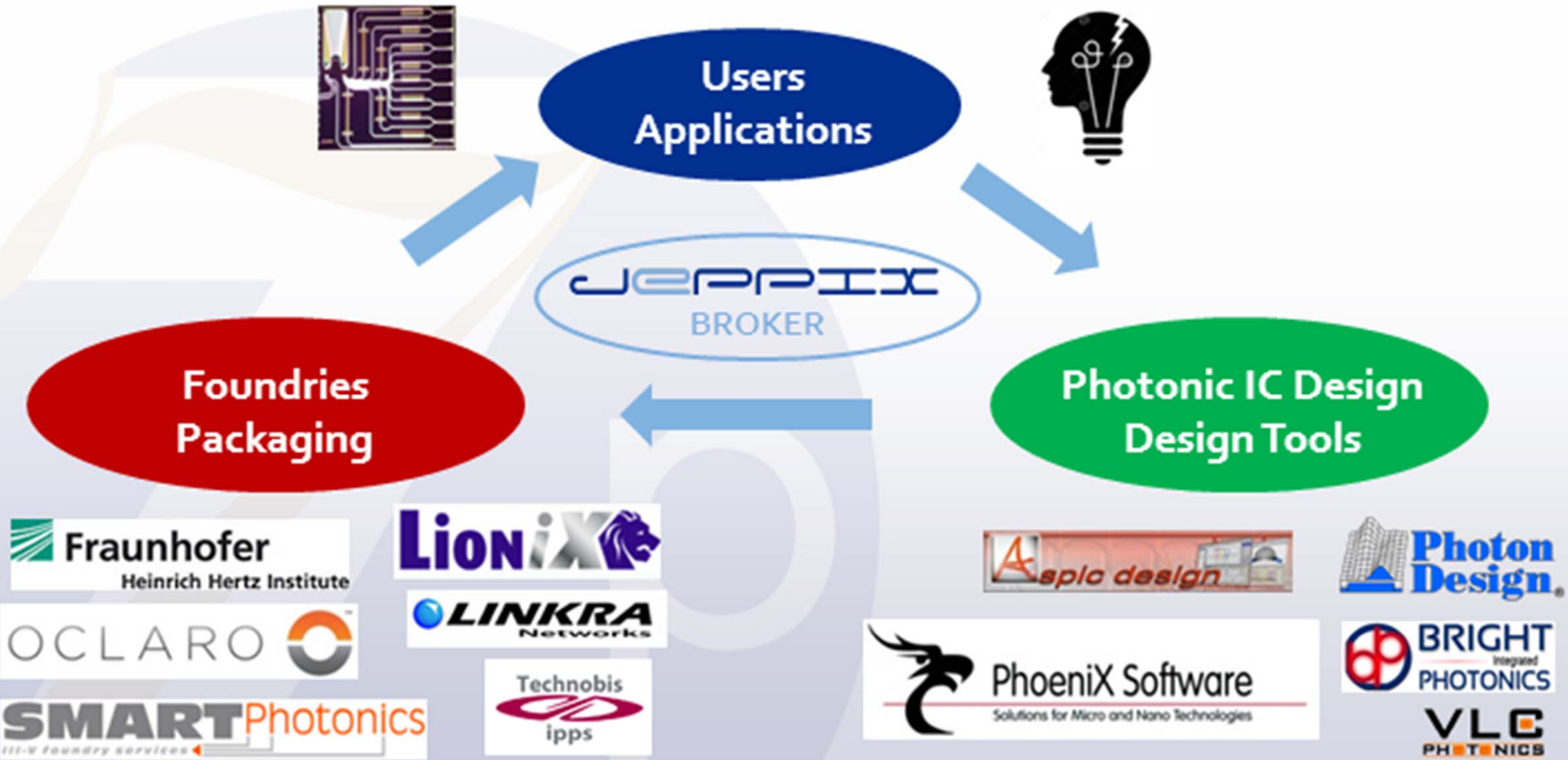


InP photonic ICs today

Electronic ICs vs. Photonic ICs

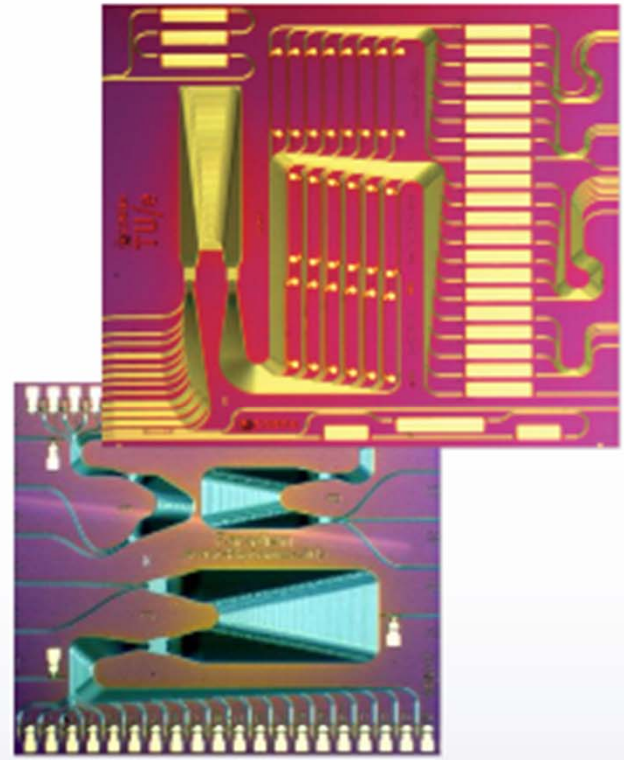
Broker: ecosystem for PIC development

✓ **Design** ✓ **Fabrication** ✓ **Packaging**



Multi-project wafer runs in photonics

- Photonic ASIC prototypes in InP MPW fabs
- Active-passive on-chip integration



✓ Integrated lasers and amplifiers

✓ High speed detectors (40 GHz, I_{dark} < 100 nA)

✓ High speed modulators (12.5 Gbps, V_{π} = 3.6V)

✓ Low-loss passives ≤ 2.0 dB/cm

✓ Tunable DBR gratings (up to 9 nm)

✓ Spotsize converters

C-band wavelength range

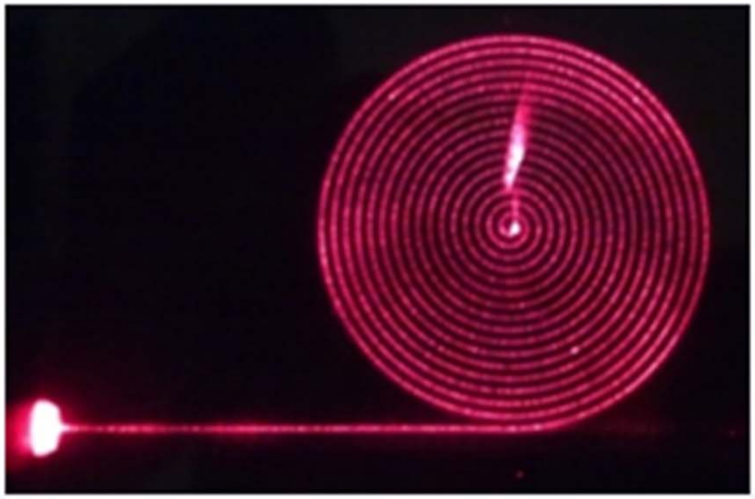
Fraunhofer Heinrich Hertz Institute

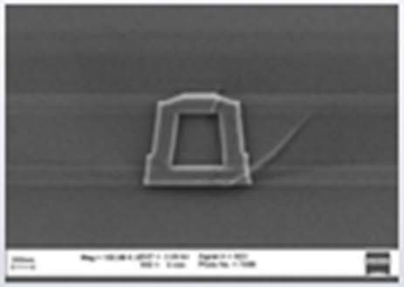
OCLARO

SMART Photonics III-V foundry services

Multi-project wafer runs in photonics

- Photonic ASIC prototypes in TriPleX MPW fab
- Low-loss dielectric waveguides :
  - silicon nitride
  - silicon oxide





✓ High Quality Passives (AWG, MZ, ring, ..)

✓ Low-loss waveguides ≤ 0.5 dB/cm

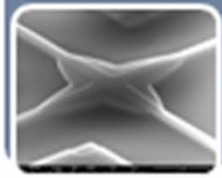
✓ Bend radii 125 µm allow real VLSI

✓ Thermo Optic Phase modulators

Visible light to IR transparency

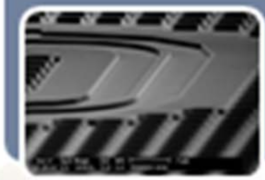
LioniX

Multi-project wafer runs in photonics



Standard Passives

Waveguide devices
Grating Couplers



Advanced passives

Waveguide Devices
High Efficiency Gratings

Heaters

TiN Heaters
Thermo Optic Tuning

Microphotonics

Low loss waveguides
Polarization insensitive

Passives	Heaters	Modulators	Detectors

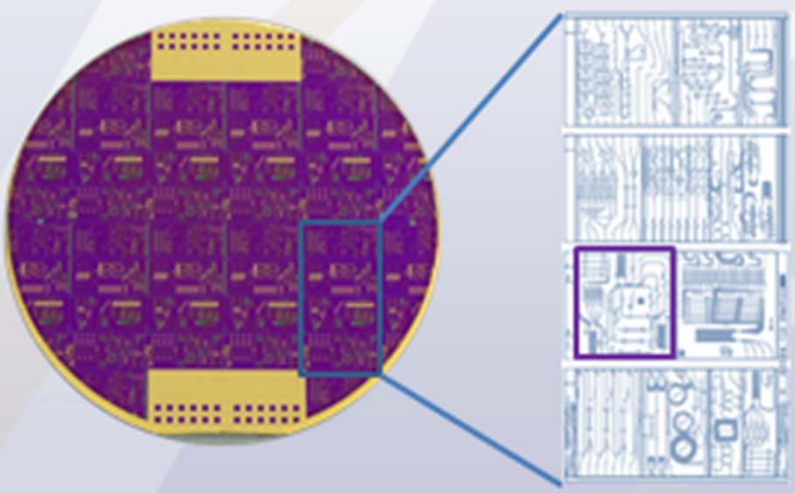
•4 etch levels in Silicon •High Efficiency Gratings	•Metal Heaters •Doped Heaters	•10Gb/s Modulators •Faster Possible	•10G detectors

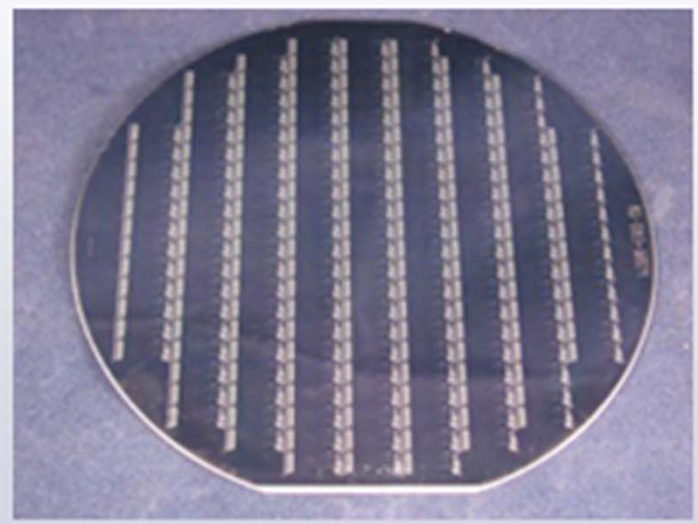
imec · cea leti · ihp · imec · cea leti · VTT · imec · cea leti

- Photonic ASIC prototypes in **Si MPW** fabs

Multi-project wafer runs in photonics

	InP	TriPleX	Si
Number of chips	5 – 10	4 – 10	10 – 50
Typical IC sizes	10 mm^2 to 36 mm^2	25 mm^2 to 250 mm^2	6 mm^2 to 100 mm^2
Costs	€ 5000 to € 40000	€ 8500 to € 16000	€ 4000 to € 140000
Per mm^2	€ 50 – € 150	€ 10 – € 50	€ 20 – € 170
Wafer size	2" – 3"	4"	6" – 8"
Chips per wafer	50 – 200	16 – 200	300 – 5000
	JePPIX	LioniX	ePIXfab





Photonic Process Design Kits (PDKs)

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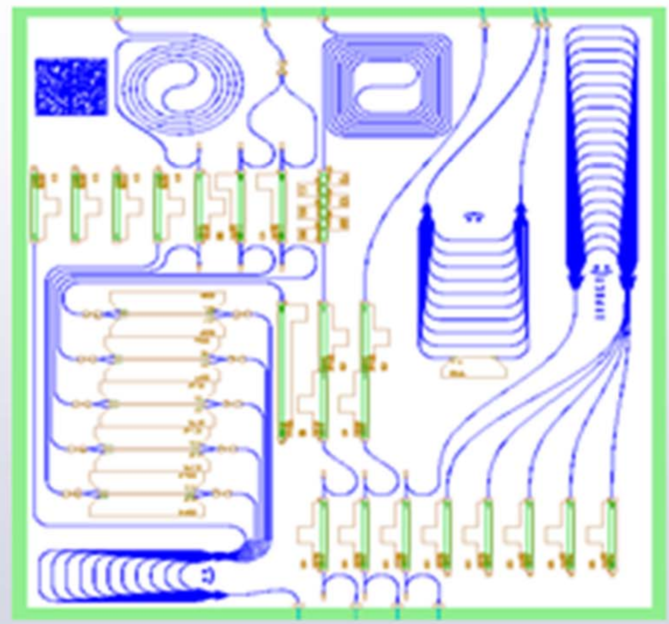
Photonic design environment

- Efficient interaction between designer and fab requires
  - Ability to check designs for process variation / functional performance
  - Ability to use existing (photonics) building blocks
  - Ability to check the design for manufacturability

- This information is available in
  - Process Design Kits (PDKs)

PDKs increase efficiency

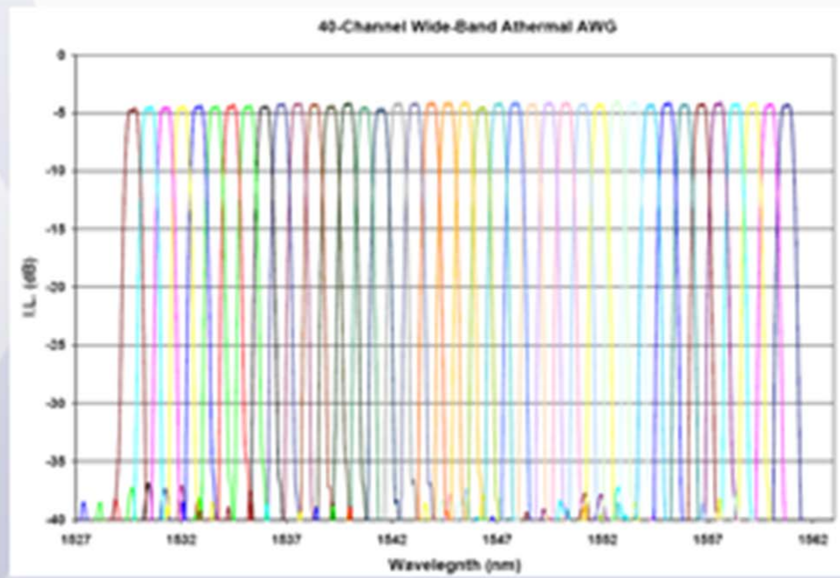
- Chip development is unaffordable if many iterations are needed for a successful design
- Ability to check functionality and process design rules can make complex design successful at the first run
    - For a simple chip, smart designer can keep track and avoid mistakes.
    - For complex photonic chip, it is difficult to keep track of all the variable without automated design environment



Photonics ≠ CMOS

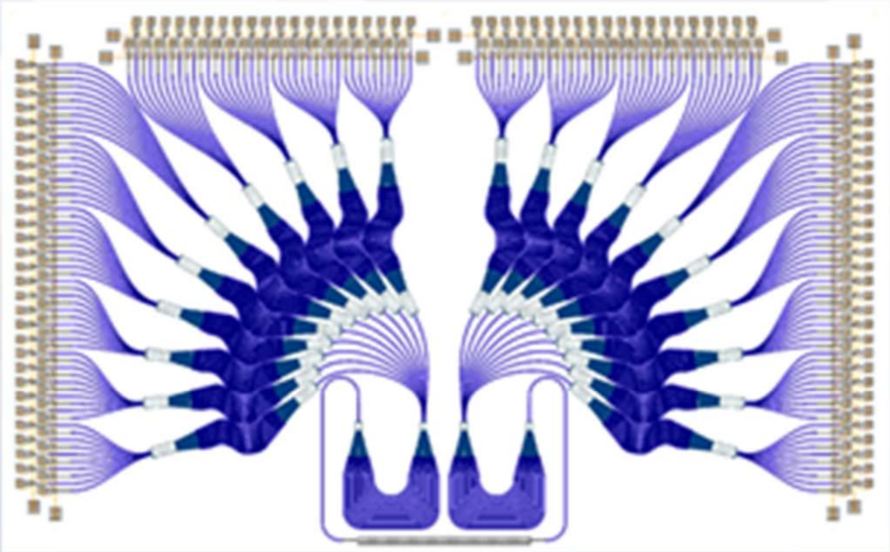
- Wafer volume <<1% of CMOS
- Typical line width : 0.2 .. 3 micron
- Current process tolerances (too) high
- “RF-like” or “analog” behavior
    - Telecom C-band is 1530–1565nm = ~193 THz

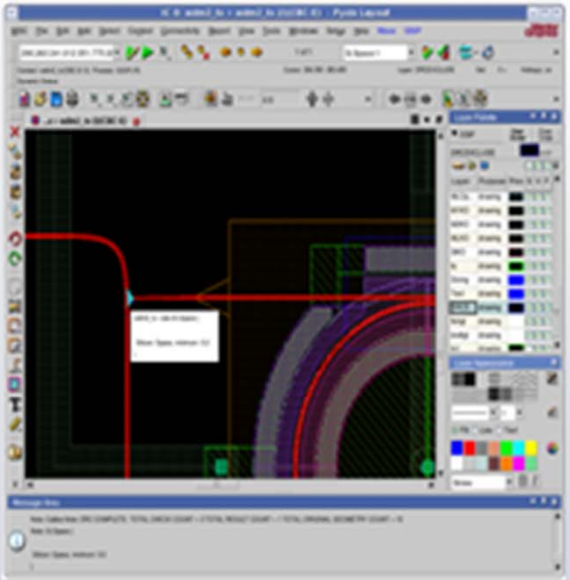
40 channel integrated optical multiplexer with a channel spacing of 100 GHz for telecom
Courtesy of Kaiam Corporation.



Photonics ≠ CMOS

- "RF-like" or "analog" behavior requires:
  - Accurate and flexible definition of shapes (all angle)
  - Control of phase (differences)
  - Dedicated photonics simulation routines
  - Libraries with parametric photonics building blocks
  - Connectivity and "smart" routing routines





Photonics ≠ CMOS

- Fabs are using Electronics Design Automation (EDA) tools, especially for Design Rule Check (DRC), sign-off and tape-out
- Photonics designers are using Photonics Design Automation (PDA) tools
- EDA tools are *not all* suitable
  All angle designs, shape definition, simulations, DRC
- PDA tools require *additional* capabilities
  Mature DRC, auto-routing, LVS, ORC, RET

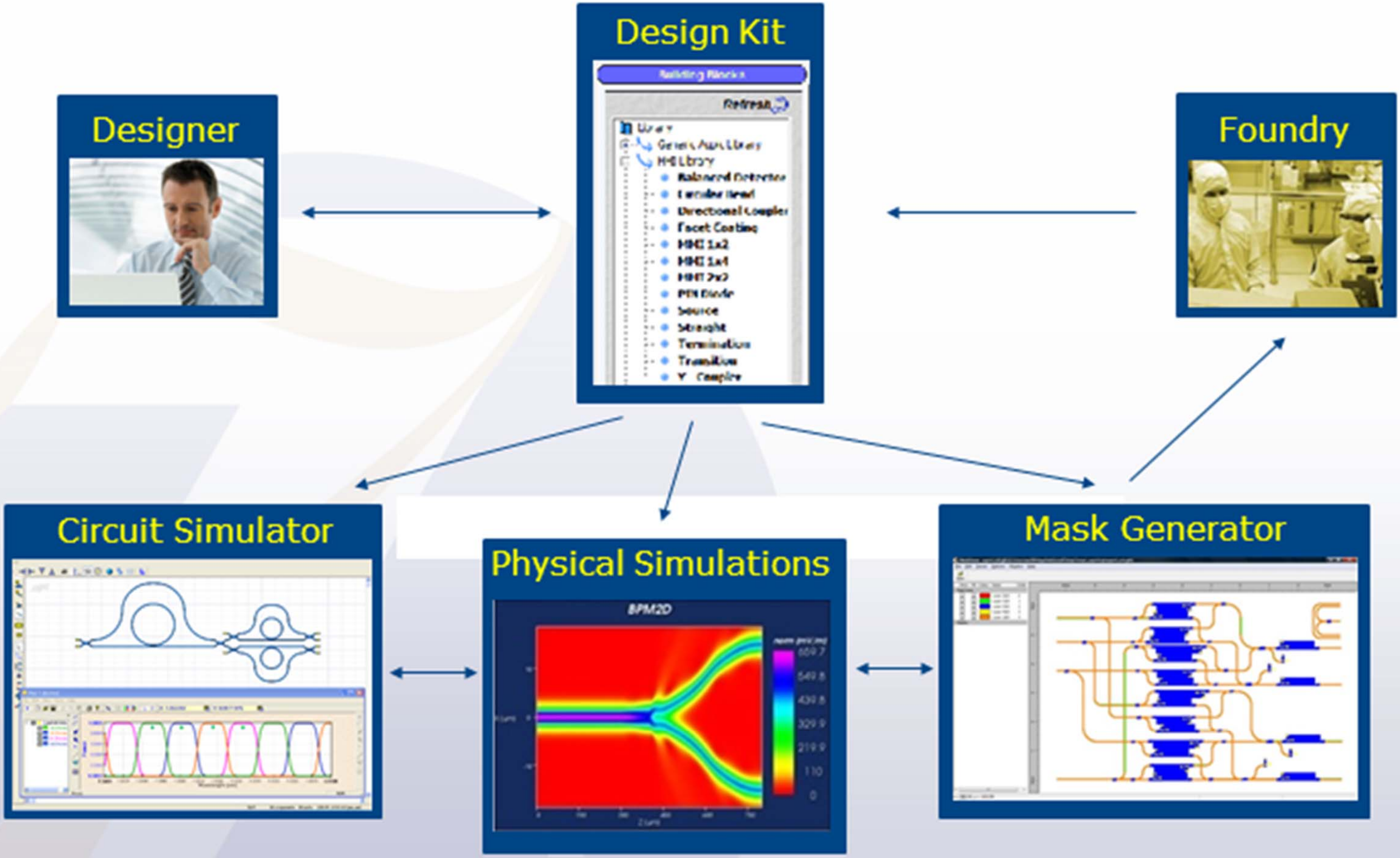
PDA & EDA design flows

EDA tools	EDA flow	PDA flow	PDA tools
	System level - system simulations	**System level** - system simulations	
Eldo	**Circuit level** - functional simulations - place and route	**Circuit level** - functional simulations - place and route	ASPIC
Pyxis Calibre	**Component level** - physical simulations - (custom) layout	**Component level** - physical simulations - (custom) layout	OptoDesigner
Calibre	**Technology level** - process simulations - DFM	**Technology level** - process flow simulations - process variability	OptoDesigner
	Equipment level - foundry solutions	**Equipment level** - foundry solutions	Living Database

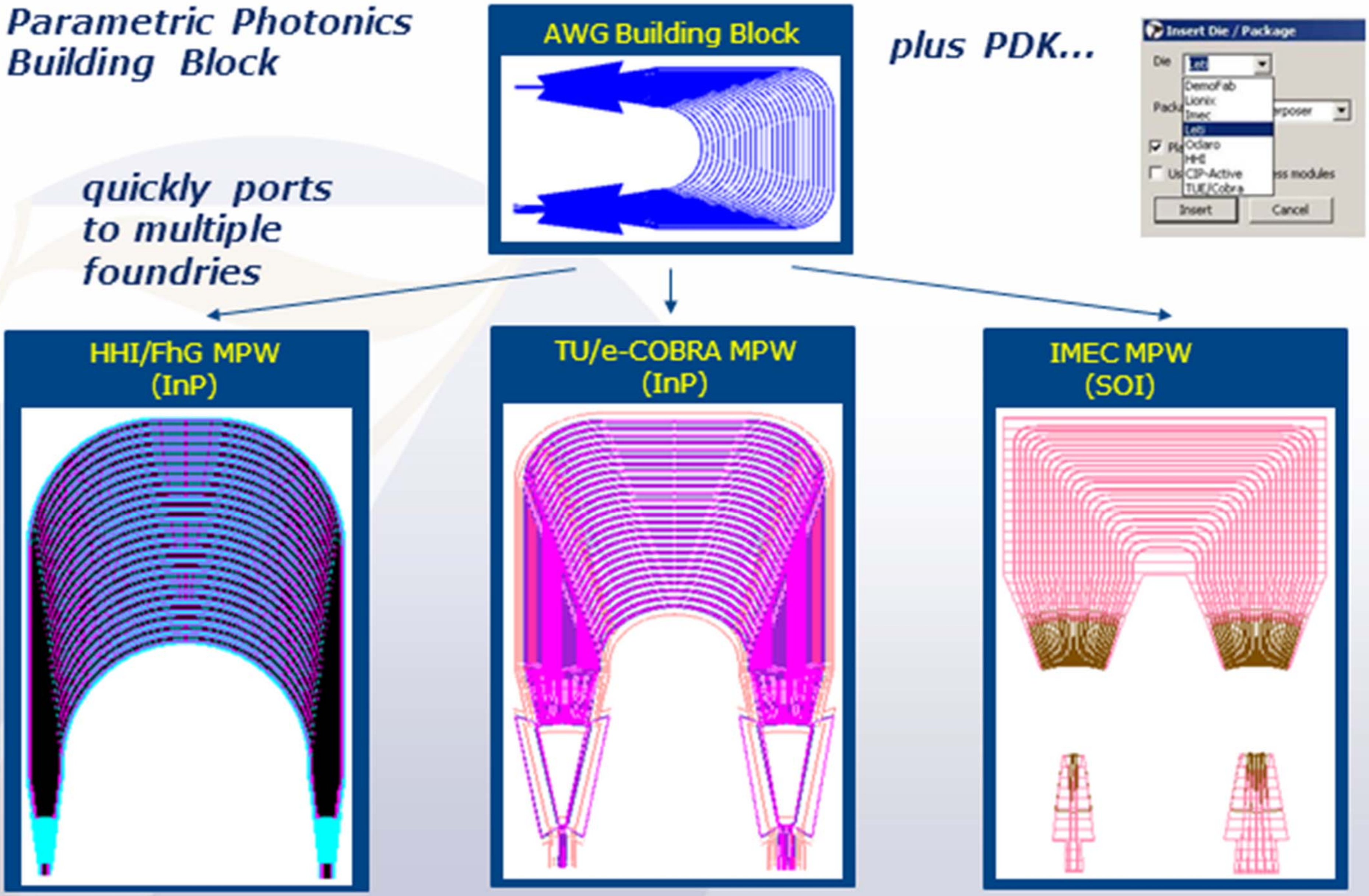
PDKs can always be used

- PDKs can be used internally or when working with an external fab or foundry
- PDKs are provided as a plug-in library for the software environment
- Software vendors are working together to further improve and standardize
  - SP-TAB
  - PDAFlow Foundation

Using a PDK in PDA style design flow

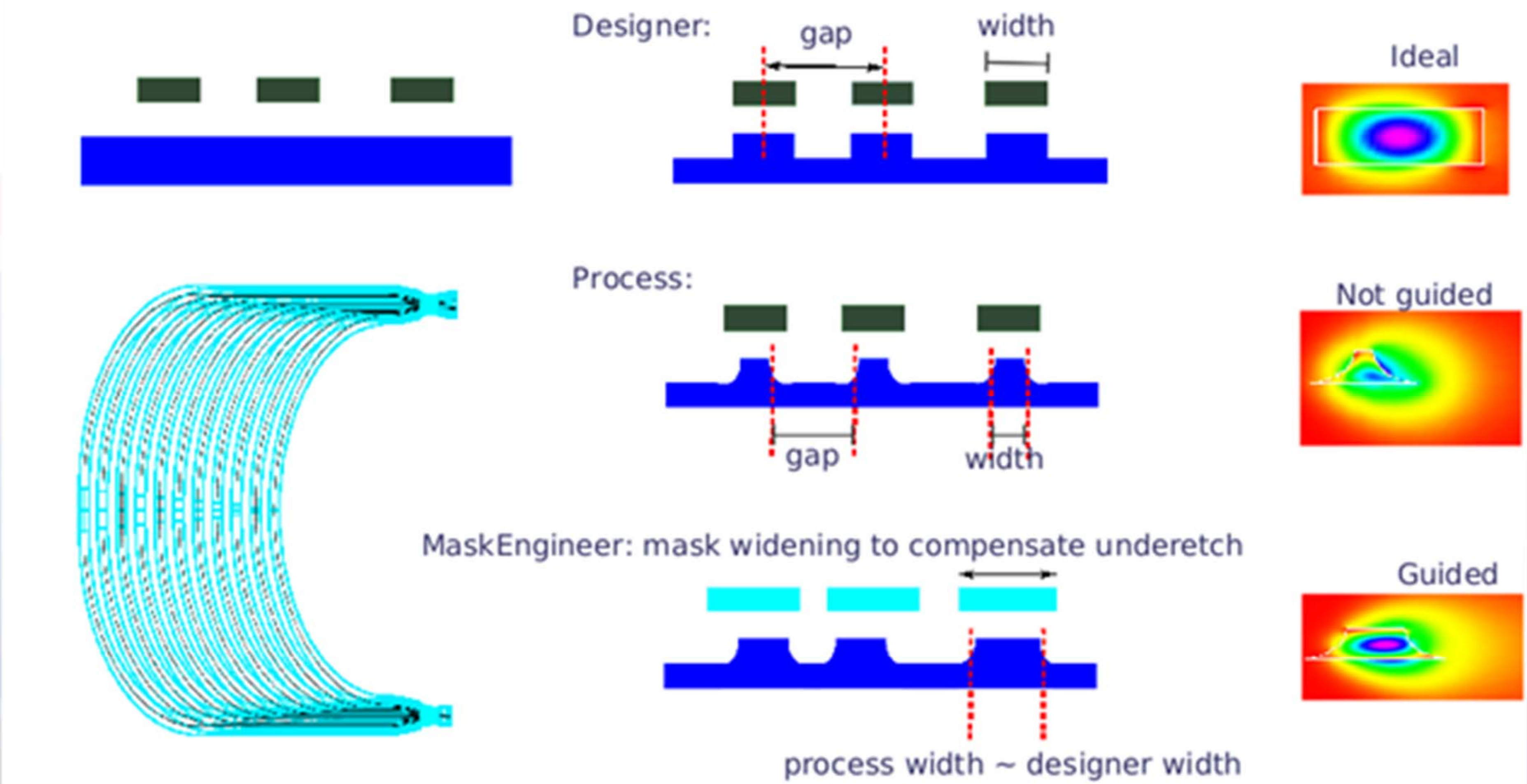


PDA style photonics design flow



PDA-style photonics design flow

- PhoeniX Software OptoDesigner 5 Photonics Design Suite integrates photonics simulations, process information and layout.



PDA style photonics design flow

- Physical and functional verification

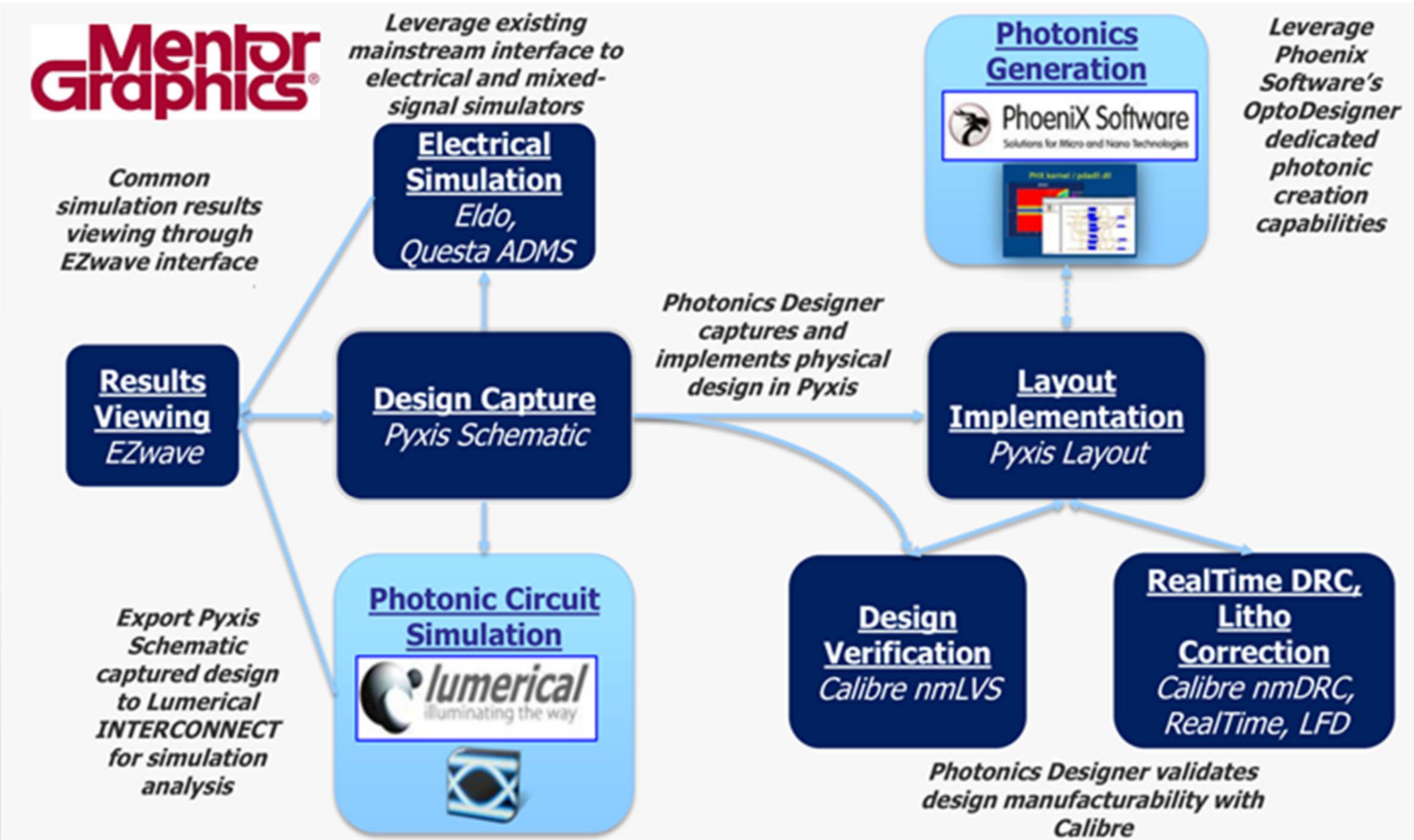
- Functional verification with OptoDesigner 5 flags that bend R is too small in original design
- When correcting for this, in/outputs need to be elastic
- Full physical DRC at GDS level with Mentor Graphics Calibre
- PhoeniX Software and Mentor Graphics working on improvements in the flow from OptoDesigner 5 → Calibre

EDA style custom design methodology

What role does the EDA style custom methodology play in Silicon Photonics?

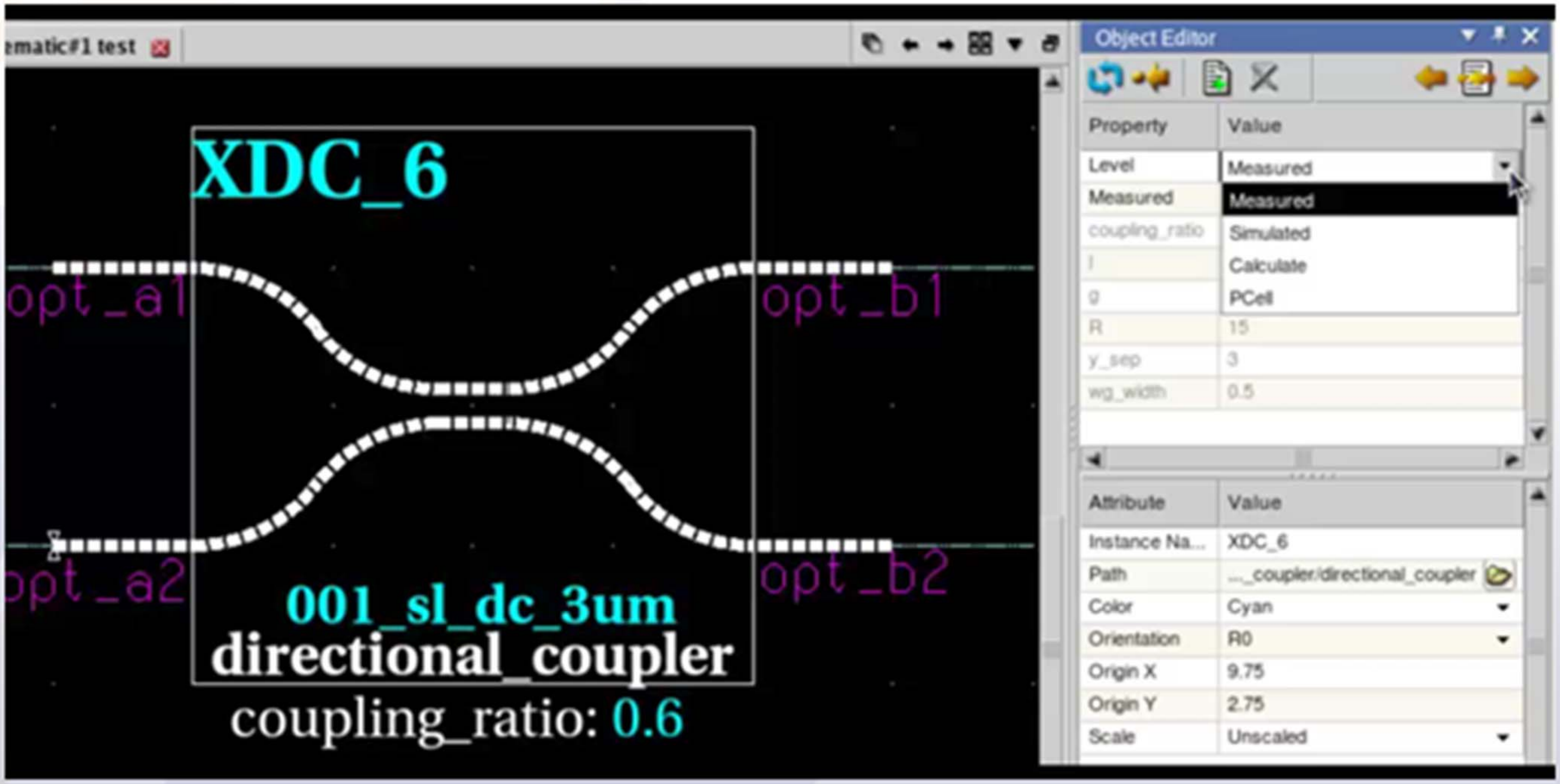
- EDA methodology has a Proven track record for:
  - Large scale custom integration of components (building blocks)
  - Multi-user / multi-site design
  - Flexible 3rd party tool and data integration
  - Existing integration to physical verification tools

EDA style photonics design flow



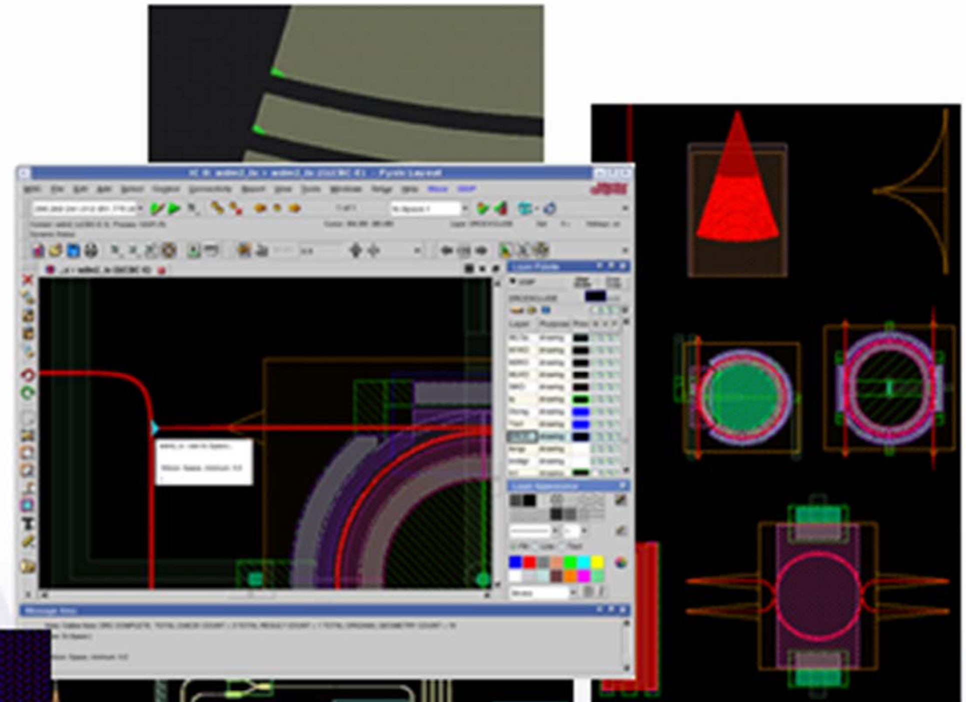
EDA style photonics design flow

- Enabling Design Intent Based Functionality
- Accelerating innovation by allowing users to configure components in terms of system parameters, not geometries



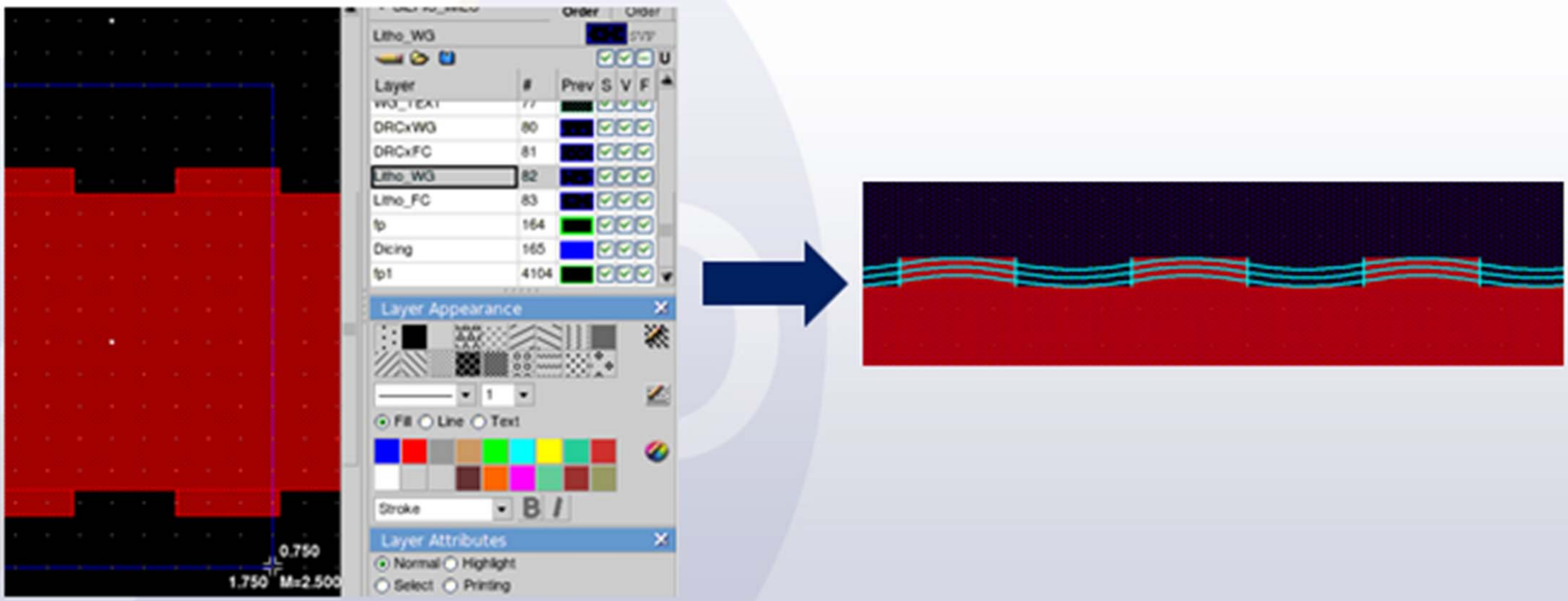
Physical verification for Silicon photonics

- Calibre Verification Platform
  - Reducing “False” DRC Errors
  - RealTime design integration
  - Recognize & extract photonic devices
  - Open detection & short isolation
  - Wave guide curvature verification
  - Lithographic Simulation



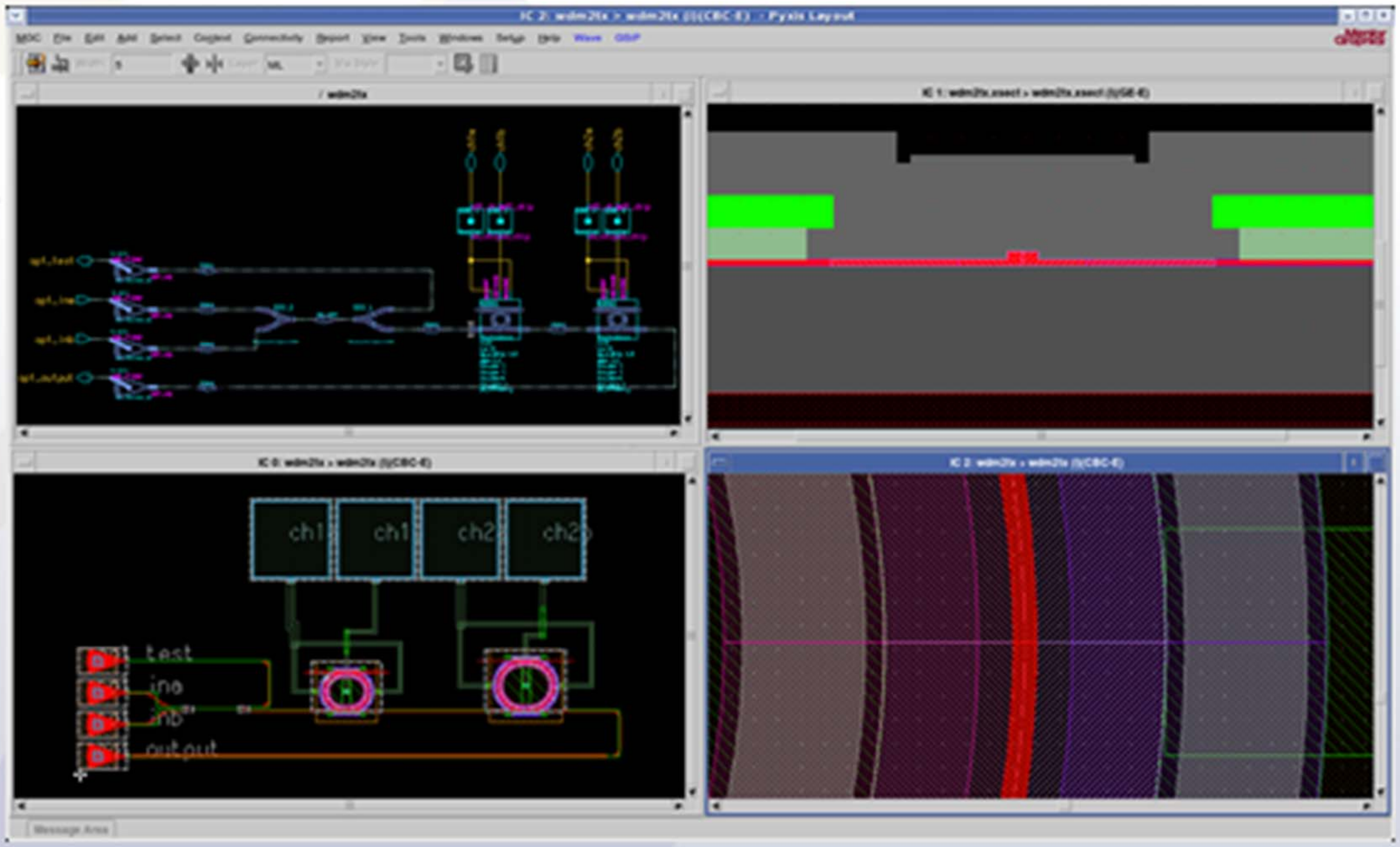
Physical verification for Silicon photonics

- LFD Example: Waveguide Bragg Grating
  - Ideal sharp edges of grating will smooth due to lithography resolution
  - This change in geometry will affect component attributes
  - Run a Calibre LFD lithography simulation directly in Pyxis Layout window with Calibre RealTime or on exported GDS/Oasis data



EDA style photonics design flow

- Reference GSiP Package
  - Mentor working with Si-EPIC program and the University of British Columbia to create a NDA neutral Si Photonics PDK
  - Demonstrates full silicon photonics design flow



PDKs compatible with PhoeniX Software

- Silicon: IMEC, CEA-Leti, VTT, IHP and OpSIS-IME
- InP: FhG/HHI, Oclaro, SMART Photonics and TU/e-COBRA
- TriPleX (SiO2/Si3N4): LioniX
- Packaging: Linkra, XiO Photonics, Tyndall, Technobis ipps and Chiral
- PDKs are typically made available through MPW service organizations
- More than 250 designs taped-out with PDKs and PhoeniX Software's design tools in the last two years

PDKs for Mentor Graphics

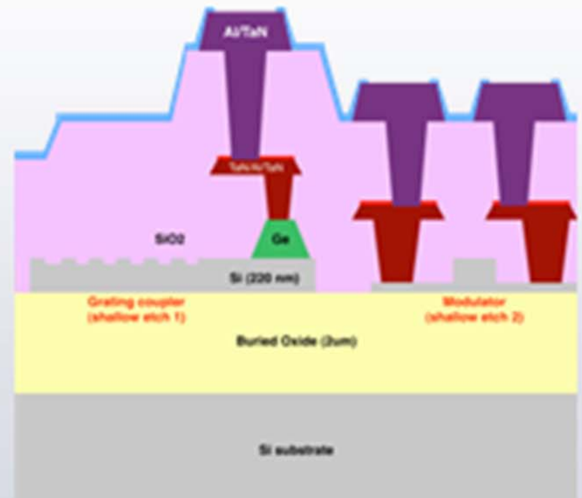
- IME and IMEC Foundry PDKs (Available through CMC/Si-EPIC)
    - "designed to train undergraduate and graduate students and postdoctoral fellows across Canada in the new discipline of ... (ICT) systems that involves miniaturization of optical components onto silicon chips" http://siepic.ubc.ca

Si-EPIC

- IMEC (PDK in development)
    - Basic PDK available – working on full flow functionality

- OpSIS (Using IME) no longer available as of May 2014
    - http://opsisfoundry.org

IME
- Passives
- Modulators
- Detectors
- Edge / grating coupling



Material Systems

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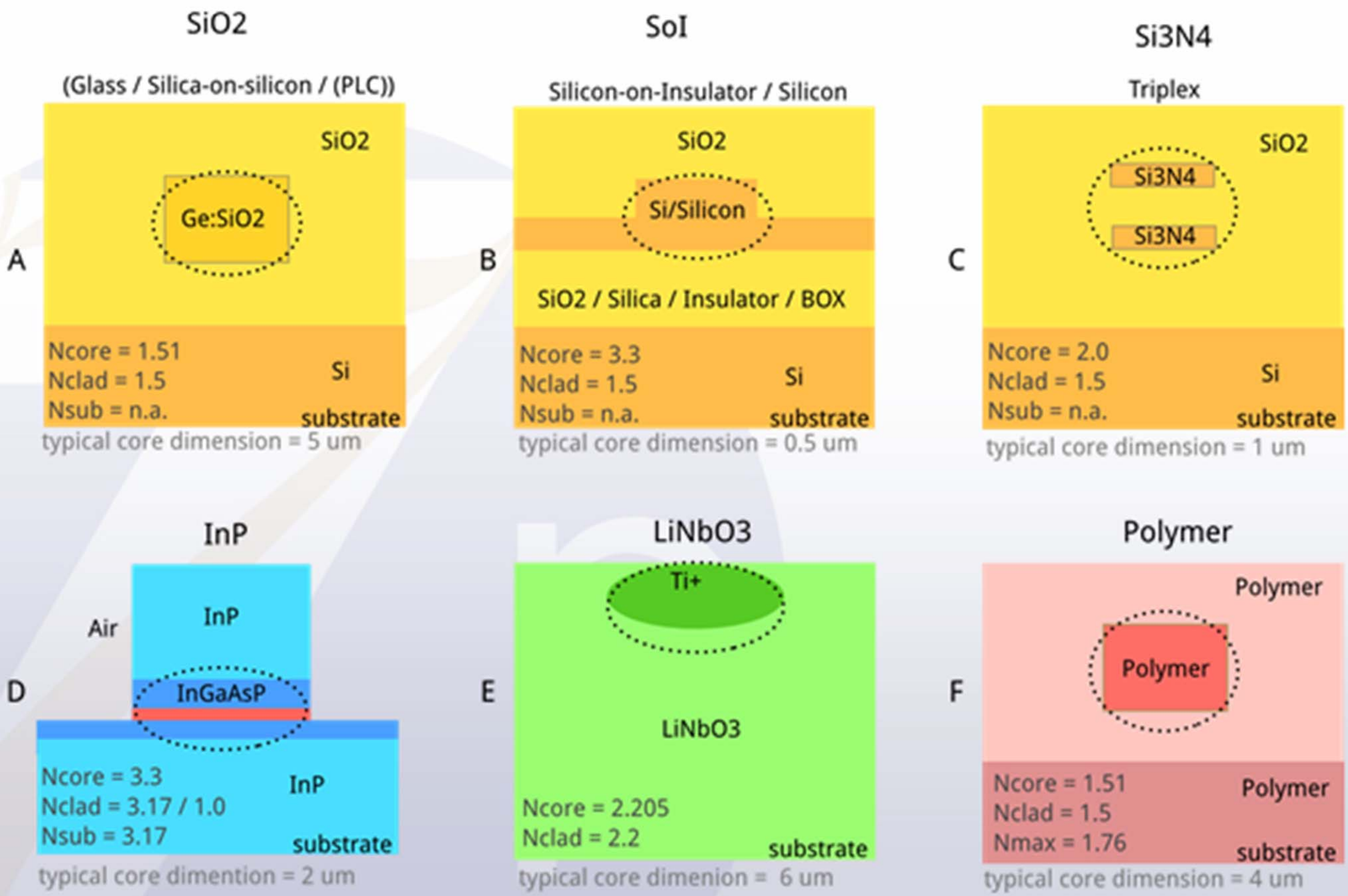
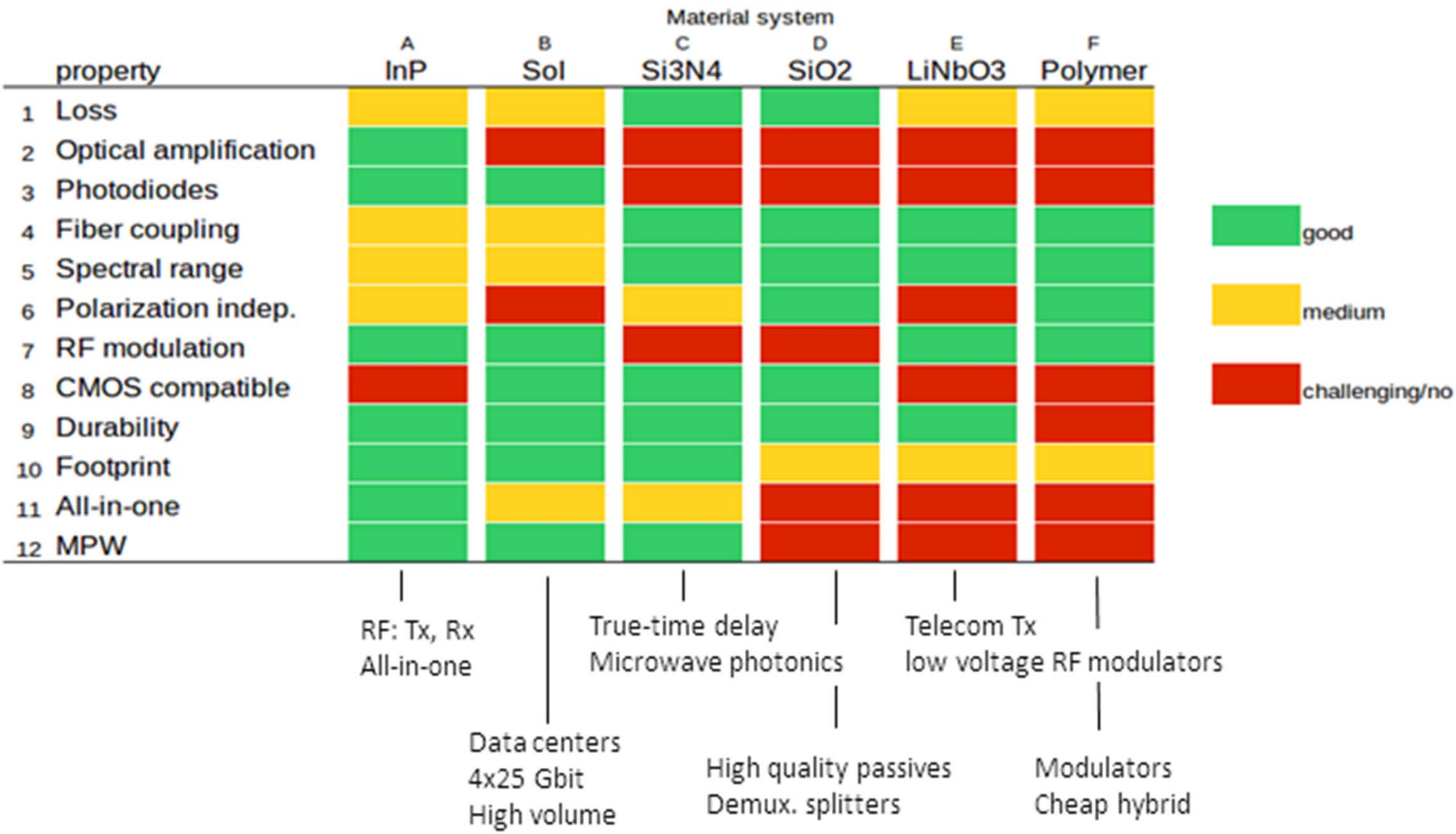
Material systems for integrated optics

Cross sectional view of the waveguides



Material systems: a comparison

A high-level functionality overview

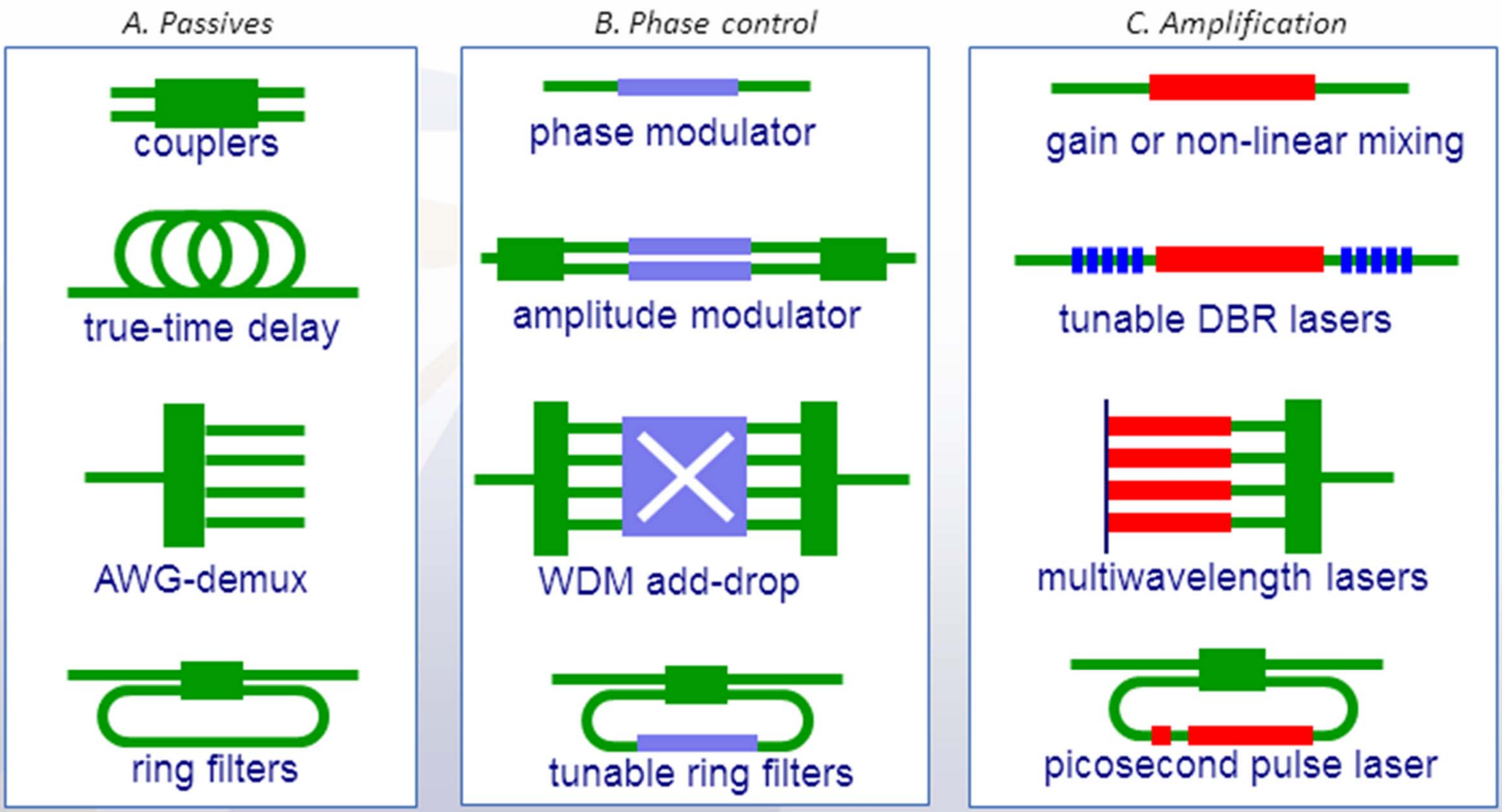


Material system: more than just material

- What is best for the final application?
- Material and more:
  - Technical merits
  - Specific foundry
  - Reproducibility
  - Post processing
  - PDK available
  - Cycle time
  - Design support
  - Packaging options
  - Cost of prototype
  - Ramp-up
  - Cost of end product

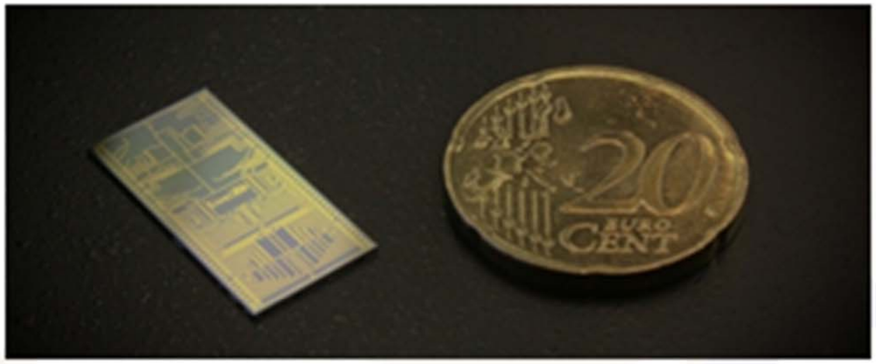
From application to material

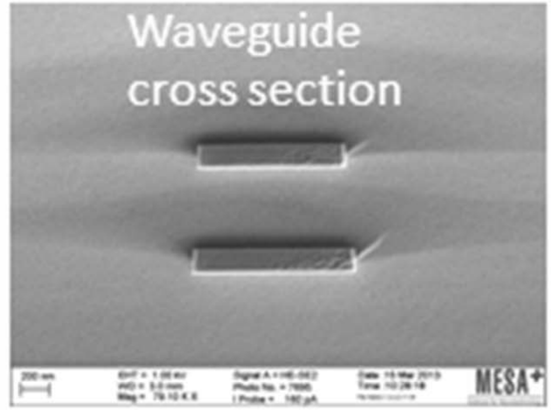
Application → Functional BB → Technological BB → Material

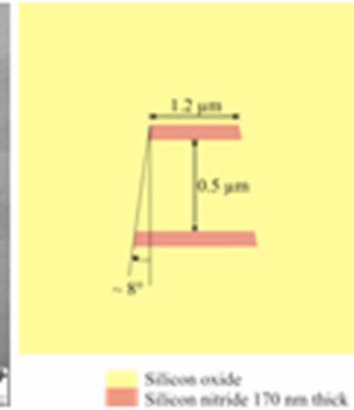


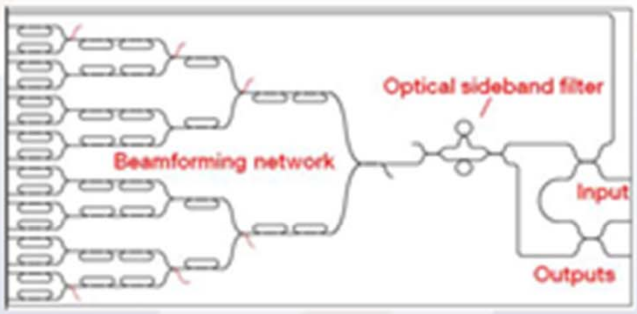
TriPleX™ technology (Si_3N_4)

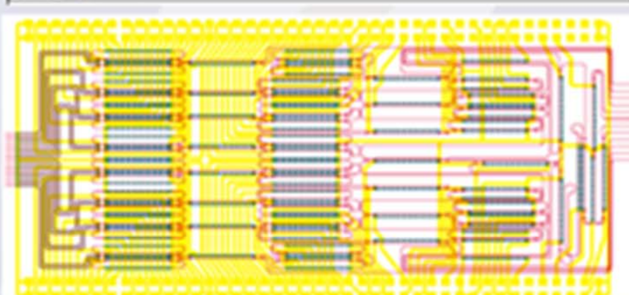
high contrast & low loss for time delays



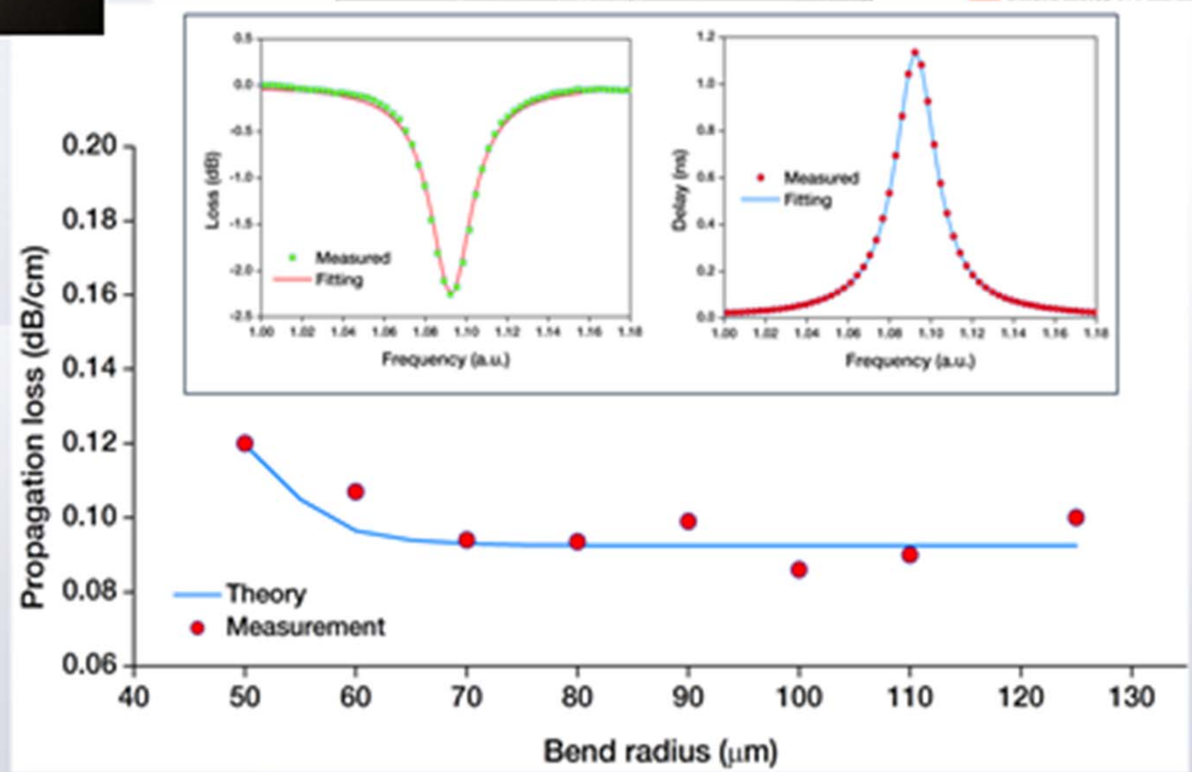






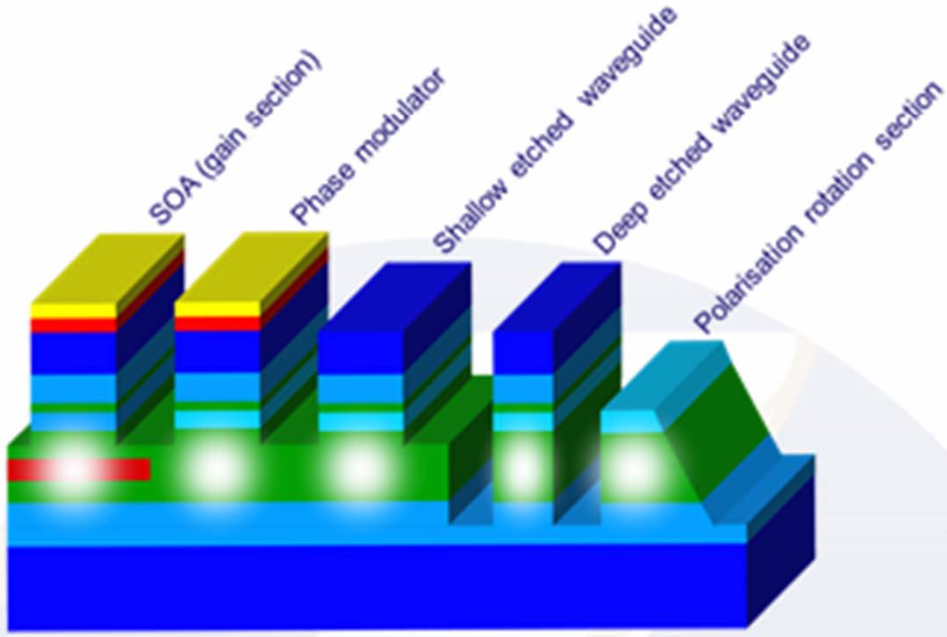


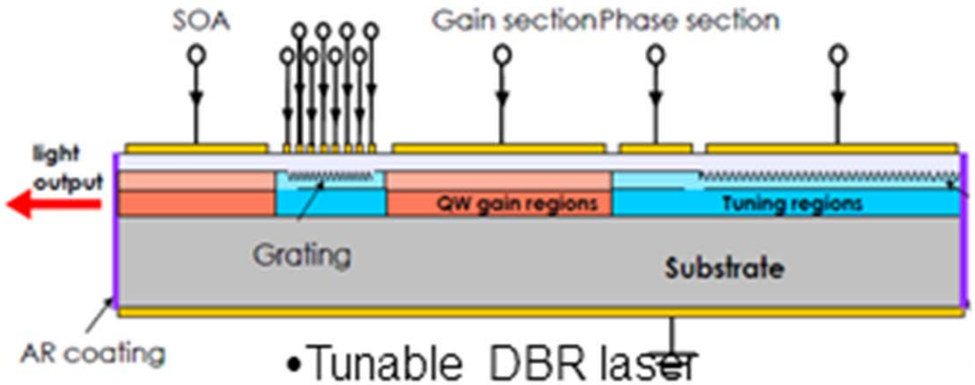
L. Zhuang, L. et al.
Optics express, 19 (23). pp. 23162-23170



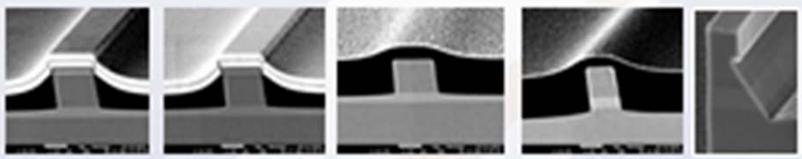
Propagation loss 0.1 dB/cm

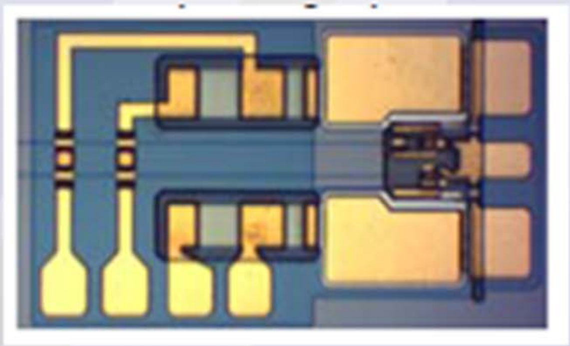
InP technology: versatile with laser





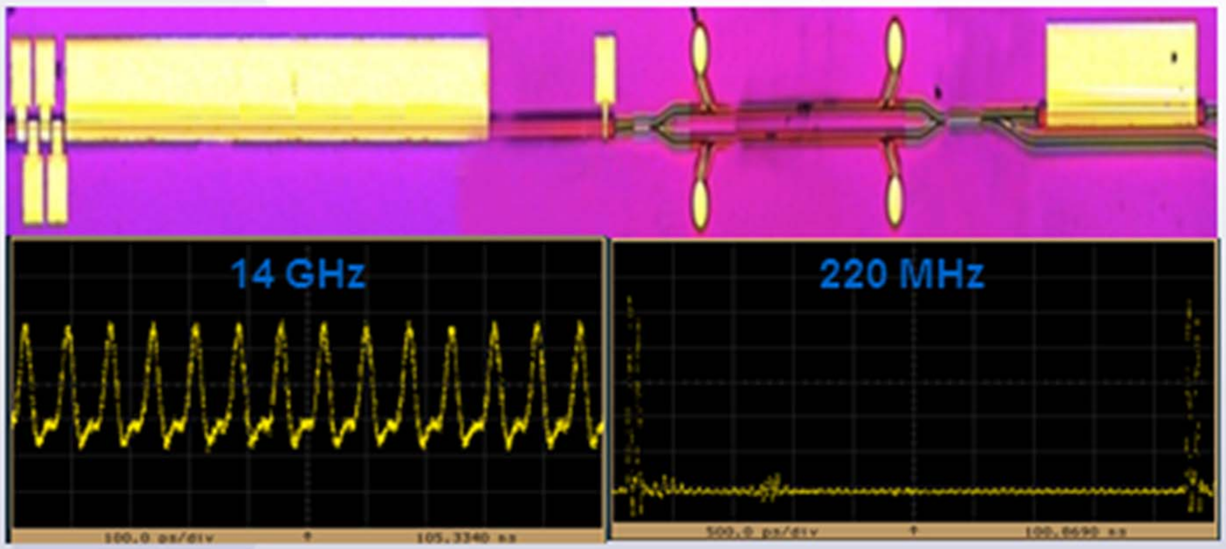
•Tunable DBR laser





•40GHz pin-PD

Variable rep-rate laser for bio-photonics



X Guo et al, ISLC, San Diego, 2012

Packaging, Scaling to Full Production and Intellectual Property

16-Sep-2014

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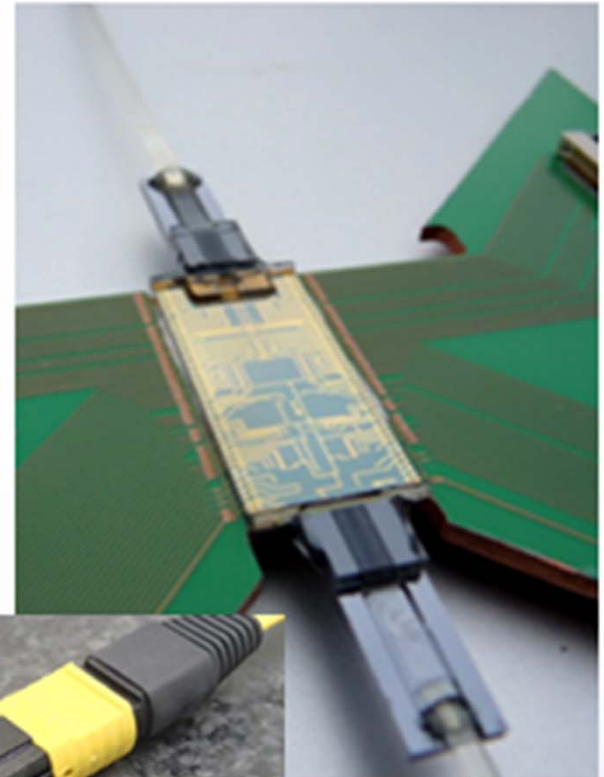
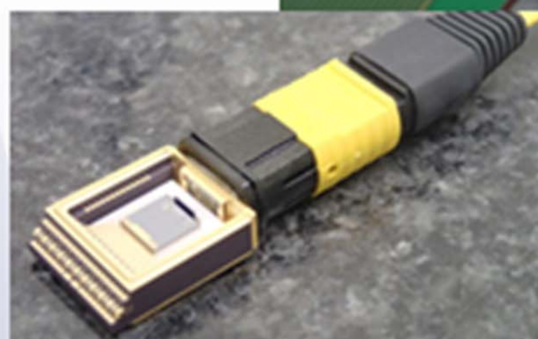
Packaging and Hybrid integration

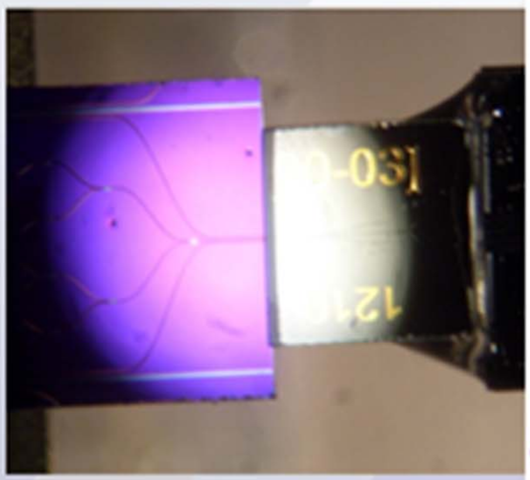
- Lot of MPW users come from R&D => Not used to measuring on bare dies.
- Both optical and electrical (RF) connections
- Design rules for packaging implemented in the design kits
- MPW foundries offer prototype packaging also
  - JePPIX => Linkra + G&H
  - ePIXfab => Tyndall
  - LioniX => XiO Photonics
- For volume production dedicated packaging foundries available in the world. Optocap, Aifotec, ...

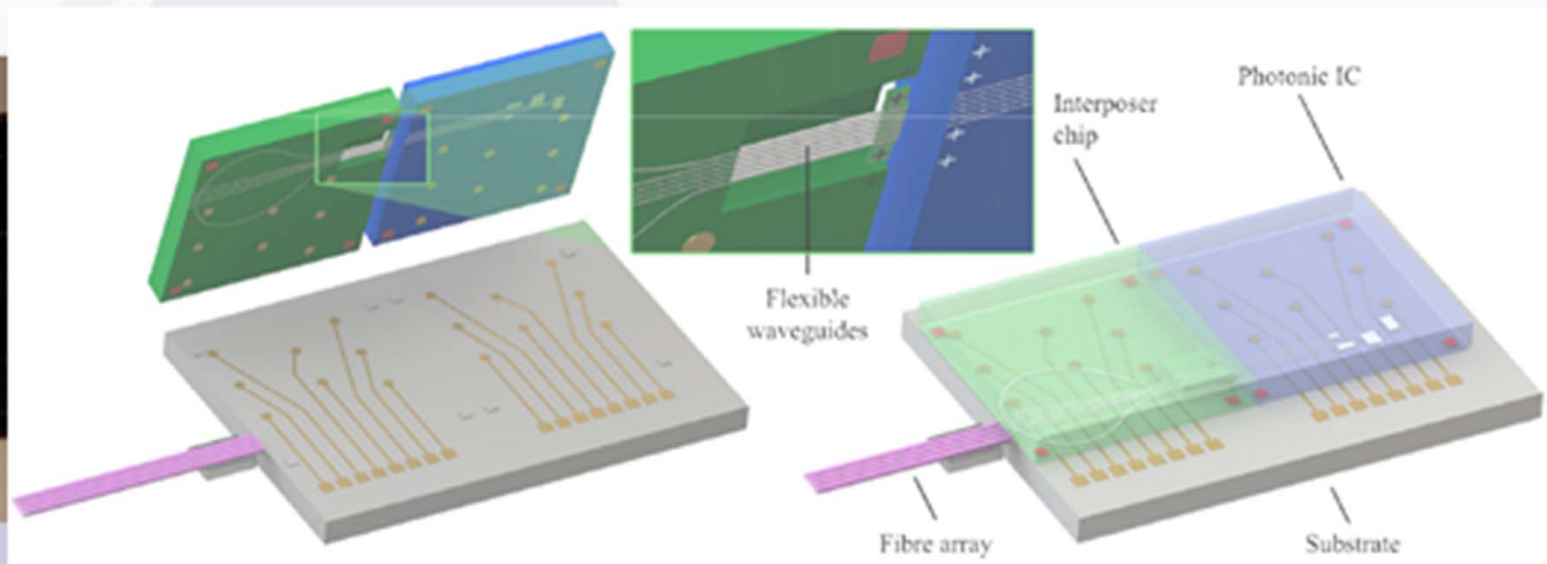




Packaging and Hybrid integration

- Heterogeneous integration not easy accessible
- Chips for hybrid integration easy accessible via MPWs
- New applications will emerge based on hybrid combinations of platforms. Use the best of all worlds.
- E.g. Create active functionality in low loss TriPleX platform => New FP7 initiative PHASTFlex (http://www.phastflex.eu)



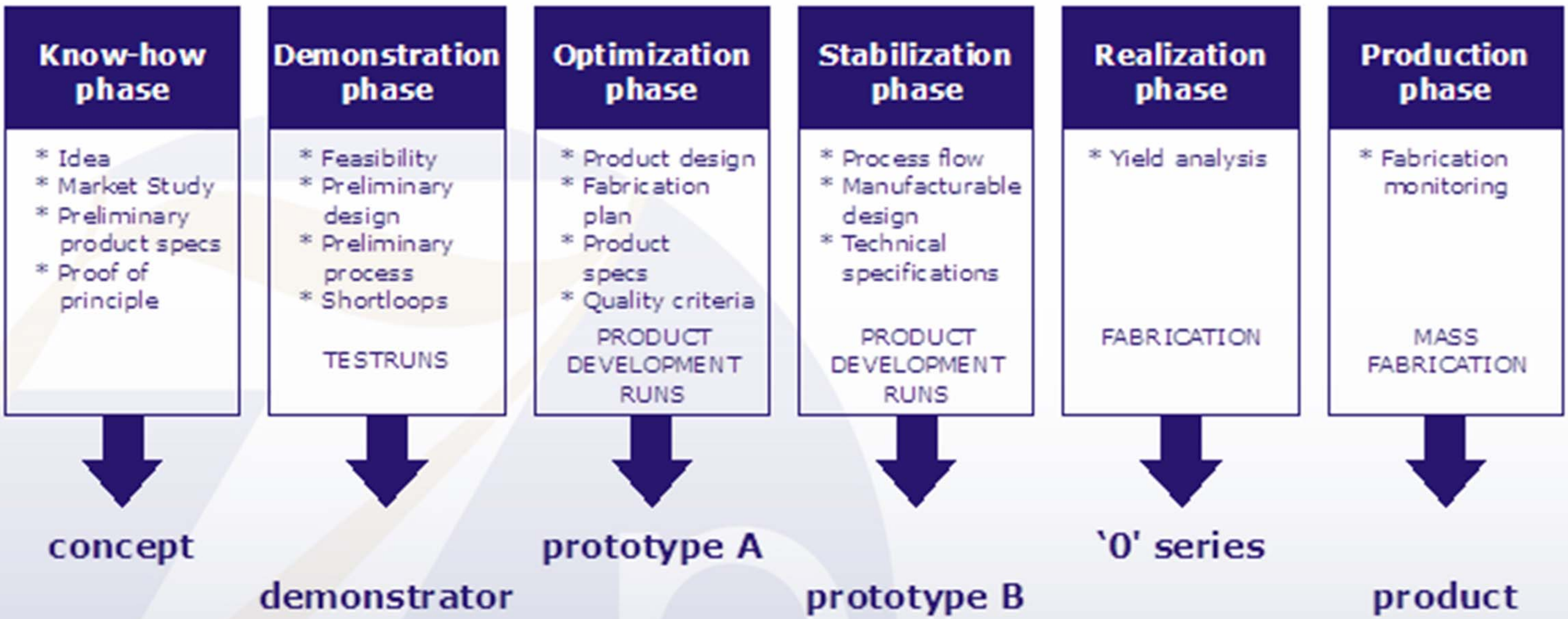


Scaling production beyond prototypes

- Initial development only requires a limited number of chips => MPW suitable for low cost an high reproducibility
- For higher volume production dedicated engineering or production runs more suitable.
- Developing in stable MPW platform prevents additional iteration when scaling up.
- Road to volume production assured by using MPW platform

Scaling production beyond prototypes

LioniX BV Strategy scheme © copyright 2002



- Prototype phases require less iterations if a stable MPW platform can be used => Designing first time right

Dealing with intellectual property

- Process validation is not done on specific device performance:
  ⇨ building block validation only
- Processes are typically owned by the foundry
- Chip design/layout is typically owned by the customer
- Specific Foundry design IP is shielded in confidential private building blocks (owned by the foundry)
- IP rules are similar to Electronics industry

Private building blocks

- The MPW participant sees a mockup (pink) within a bounding box with the name of the private building block (brown), together with his own design (red) in the viewer of OptoDesigner

- DRC checks are carried out, files for the foundry are generated, amongst which a mask file (gds), that contains a hole at the position of the private building block

- After transferring the files to the foundry, the software inserts the private mask layout of the foundry (not shared with the participant)

Full Service Design House

16-Sep-2014

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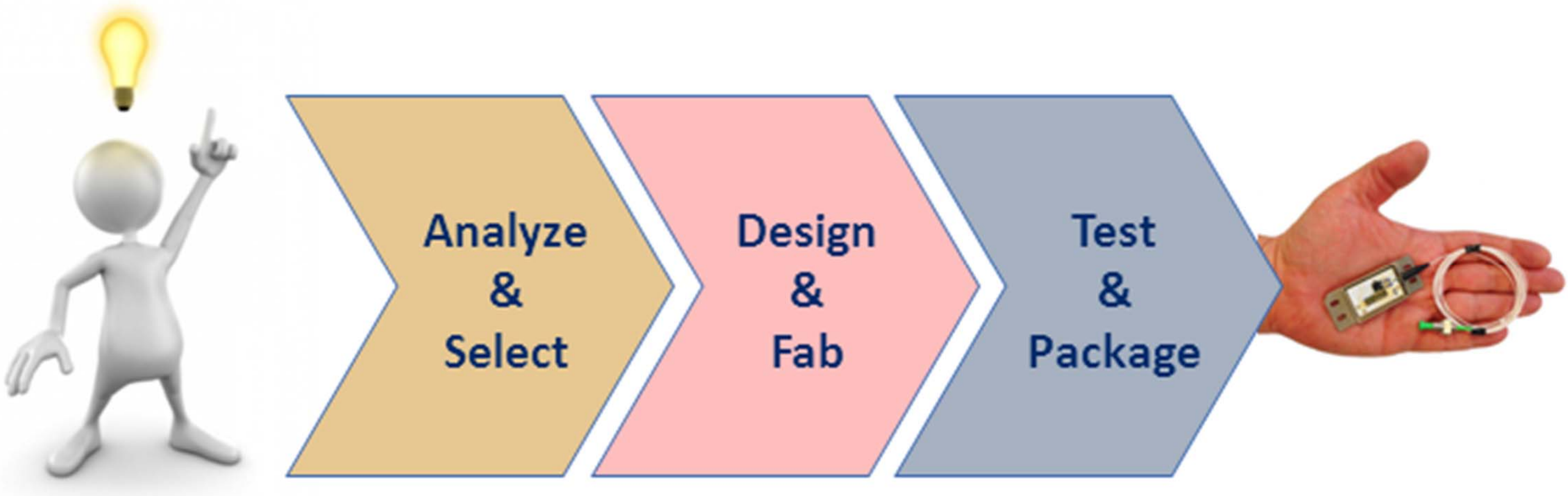
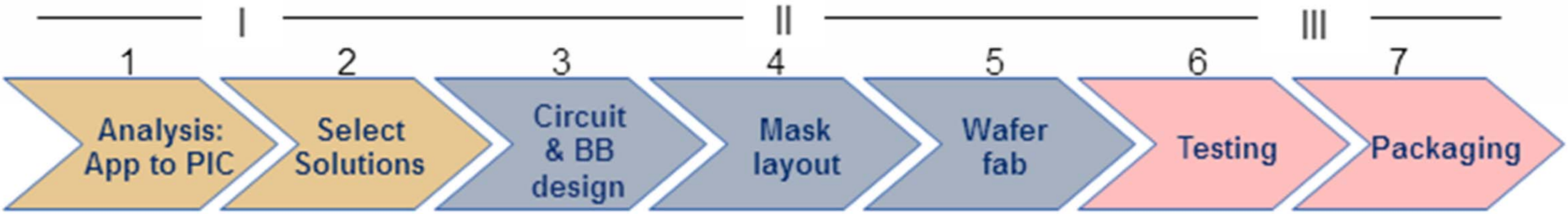
Design house supports from application idea to PIC prototype

- In 3 phases from idea to packaged PIC



Design house support 3 phases in 7 steps



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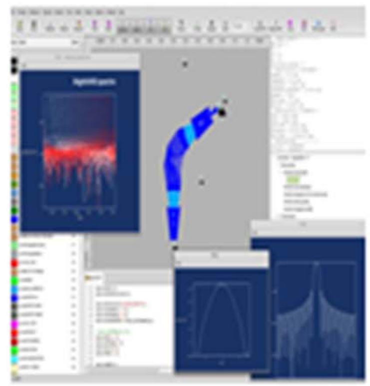

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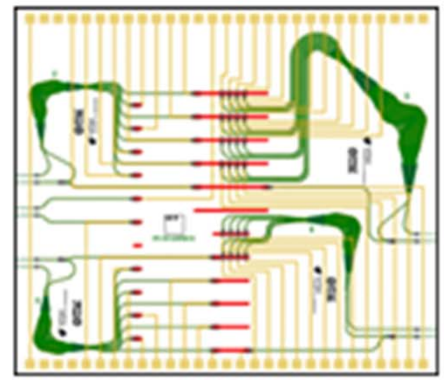

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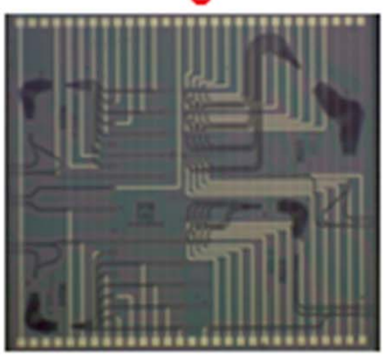

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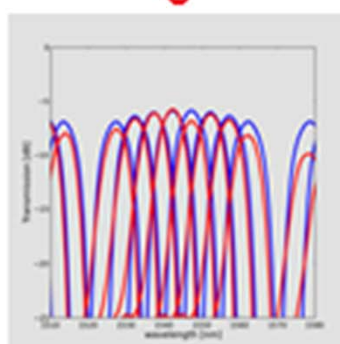

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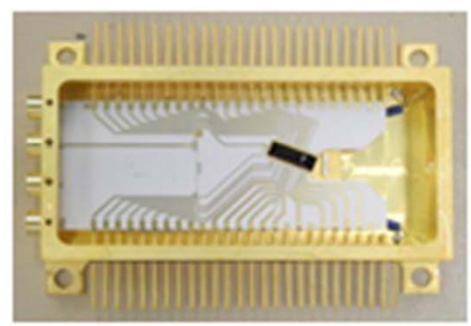

Summary

- Integrated optics is gaining momentum
  - Especially for 100Gbps, but also in many other areas.
- Developing a PIC can still be expensive…
  - MPW brings down the costs & simplifies the process to create a PIC
- Use a detailed automated PDK plus the right design S/W.
- Choosing the right material is tricky, but MPW services are available for the most important material systems.
- All MPW foundries can seamlessly scale from prototype to dedicated (custom) production runs.
- There are a good number of packaging options
- And hopefully with all these efforts together, the field of integrated optics can gain even more momentum.

Thanks!

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It’s Time for Questions

You can submit a question using the question tool on your screen.

7pennies Consulting · Bright Photonics · JePPIX · LioniX · Mentor Graphics · PhoeniX Software a LIGHTWAVE LiveWebcast

Thank you for attending.

More questions?

Contact:

Erik Pennings at erik@7pennies.com

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